

HOMEWORK 1.**Due: Thursday, February 12, 2003 at 5pm in 558 Cory****This is an individual assignment!**

The goal of this assignment is to get familiar with the class technology. It is fairly long – knowledge of some scripting language (like Perl) could be useful.

1. Spice models

Use the BSIM3v3 (HSPICE Level 49, PSPICE Level 7) model to characterize a 0.18 μm CMOS process (TSMC); parameter files are on the class home page.

- a) Determine the threshold voltage V_{Th} , for the NMOS and PMOS devices (for $V_{BS} = 0$, $L = 0.18\mu\text{m}$ and $W = 1\mu\text{m}$), by extrapolating from the I_D - V_{GS} curve at low V_{DS} . Explain your circuit setup. How does this result compare to values reported in the model file? Also, determine the body-effect parameter.
- b) Determine the subthreshold slope factor S for the NMOS and PMOS devices (at $V_{DS} = 1.8\text{V}$, room temperature). Determine the leakage currents at $V_{GS} = 0\text{V}$. Repeat it at a lower temperature $T = 77\text{K}$.
- c) Determine the effects of channel length L on the threshold voltage V_{Th} between 0.18 μm to 2.0 μm . Draw V_{Th} of the NMOS and PMOS as a function of L (for $V_{DS} = 1.8$ and 1.2 V).
- d) Determine the effects of drain-source voltage V_{DS} , on the threshold voltage V_{Th} between 0 and 1.8 V. Draw V_{Th} as a function of V_{DS} (for $L = 0.18\mu\text{m}$). Explain your measurement setup. What is the measured DIBL factor?

2. RC modeling of CMOS gates.

The goal is to explore the equivalent RC models of CMOS gates.

- a) Resistance from static DC characteristics: By plotting the I_D - V_{DS} characteristic for $V_{GS} = 1.8\text{V}$ using HSPICE, compute the average resistance of the NMOS ($L = 0.18\mu\text{m}$, $W = 1\mu\text{m}$) pull-down switch in an inverter during the transition.
- b) Using Hspice, plot the t_{pHL} and t_{pLH} for an inverter with fanouts of FO = 1, 2, 4, 8. Use the simulation setup as shown in Fig. 2.b. Each inverter is sized equally, but drives fan-out of its copies. Repeat the simulations for a 2-input NAND, and plot t_{pHL} and t_{pLH} . Use 10-90% rise times at the inputs of 80ps, and the first inverter in the chain has $W_N = 1\mu\text{m}$ and $W_P = 2\mu\text{m}$. Find the logical effort of a NAND from these simulations.
- c) Analytically derive the inverter delay dependence on the input slope. Assume the simplest model – where the drain current is linearly proportional to V_{GS} .

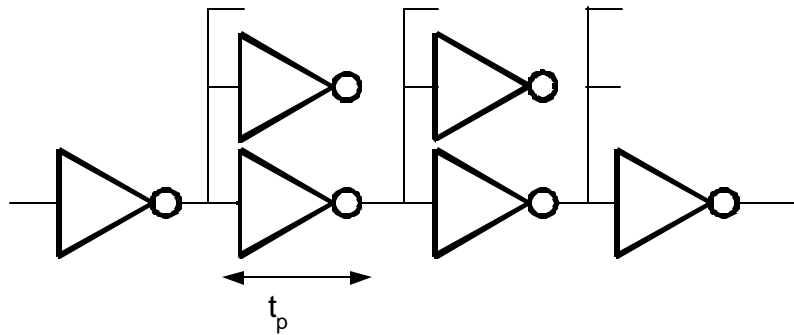


Fig. 2.b.

- d) Let's try to estimate equivalent resistance and capacitance of an inverter during switching, using the setup from Fig. 2.b. Replace the output load of the second inverter in the chain with a capacitor. Determine the capacitance C_{eff} that results in the same average delay for this inverter as a fanout-of-4 loading inverter. Normalize the input capacitance to a $2\mu\text{m}/1\mu\text{m}$ inverter. Then, with this linear capacitor in place, find the equivalent output resistance of the first inverter, R_{eff} , that results in the same average delay during switching, and compare this result to value obtained in part a). Comment on possible differences. How could you distinguish the impact of gate and diffusion capacitances?

3. Transistor sizing

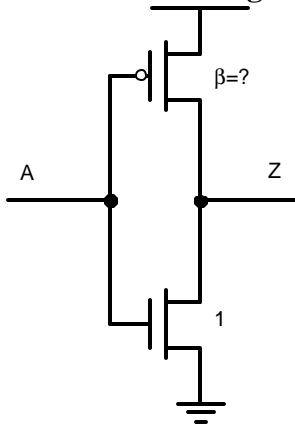


Figure 3.a

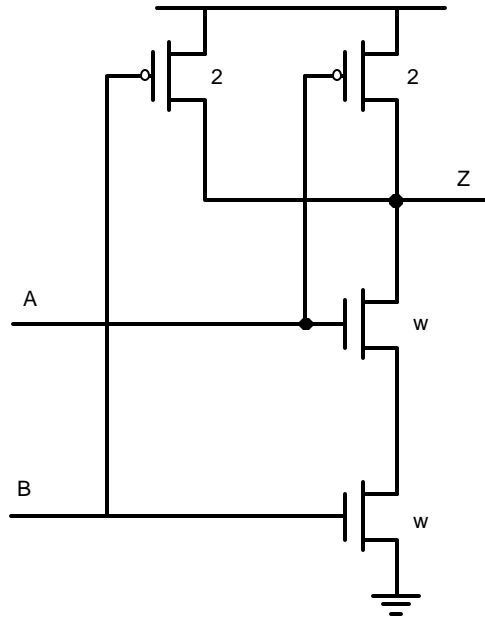


Figure 3.b

- Using SPICE find the β ratio that makes the inverter in Figure 4.a symmetrical. Use the $0.18\mu\text{m}$ CMOS process (TSMC) from the class web page.
- Using SPICE, find the required width (W) for the NMOS transistors in Figure 4.b such that the equivalent resistance of the pull-down network is the same as the equivalent resistance of the pull down network in Figure 4.a. Use 3 input configurations:
 - Both inputs A and B switch simultaneously
 - $B = 1$ and only A switches
 - $A = 1$ and only B switches

Report the corresponding W for each of the 3 situations. Explain your results – compare them with hand analysis.

4. Alpha-power law model

Let's examine the alpha power law for the drain current:

$$I_D = K(V_{GS} - V_{Th})^\alpha$$

- a) We will try to extract the parameters V_{Th} and α from SPICE simulations. Assume $W_N = 1\mu\text{m}$, $W_P = 2.2\mu\text{m}$ and get 10-15 simulation points. Use then Matlab to determine K , V_{Th} and α (hint: use the `lsqcurvefit` function). Determine the parameters for both NMOS and PMOS transistors.
- b) By setting $\alpha = 1$, find the V_{Th} that corresponds to linear dependence of current on V_{GS} .
- c) Using the alpha power law model, find the analytical expression for the delay of a CMOS inverter driving a capacitive load. Using the setup as in Problem 2, extract new values of parameters V_{TH} and α that fit the best your analytical model for delay. How do they compare to parameters extracted from current fitting?