

HOMEWORK 3.**Due: Tuesday, March 30, 2003 at 5pm in 558 Cory****This is an individual assignment!****Problem 1. Logical effort.**

a) We have shown in the class that optimal stage effort is about 3.7 (rounded up to 4) for static complementary CMOS circuits. Find the optimal stage effort for domino logic. Keep in mind that domino logic stage essentially has two gates, where the static inverter is skewed.

If you have a static complementary CMOS design and would like to re-design it in domino logic in order to speed it up, would you prefer to use more or less logic levels than in static implementation?

b) Consider two designs of dynamic 8-input OR gates:

- Design A consists of two 4-input domino OR gates, followed by a 2-input domino OR.
- Design B consists of a two dynamic 4-input NOR gates, followed by a 2-input high-skewed static NAND.

Assume that these dynamic gates are not at the beginning of the pipeline, so you can eliminate the foot switch.

Your task is to compare the speed of these two designs.

- Which design is faster if the output capacitance is equal to the input capacitance?
- Which design is faster if the output capacitance is 16 times larger than the input capacitance?
- Repeat this exercise for the design of an 8-input AND with fanouts of 1 and 16.
- Can you draw a conclusion when would you build logic into the static gates that follow dynamic gates?

Problem 2. Dynamic voltage scaling.

Consider a FO4 inverter chain of a length of 20.

- Using Hspice simulations in 0.18 μm technology, plot its power dissipation vs. operating frequency when the cycle time changes from 20FO4 to 100FO4, with constant supply voltage $V_{DD} = 1.8\text{V}$. The unit inverter is sized 2 $\mu\text{m}/1\mu\text{m}$ with minimum channel lengths.
- Repeat the simulation from a) for the same inverter chain in the same frequency range, but this time adjust the supply voltage for each frequency such that the power dissipation is minimized. Plot this curve on the same diagram with part a).
- Repeat the simulation from a) for the same inverter chain in the same frequency range, but this time adjust the substrate biasing while keeping the constant supply $V_{DD} = 1.8\text{V}$. Plot this curve on the same diagram with parts a) and b).
- Repeat the simulation from a) for the same inverter chain in the same frequency range, but this time adjust both the supply and substrate biasing to minimize power. Plot this curve on the same diagram with parts a), b) and c). How do you determine optimal supplies and thresholds for given frequency in this case?

- e) Using Hspice and α -power law modeling results from Homework #1 (including body effect factor) and Matlab (or other tool of your choice) find the analytical expressions for energy and delay of this inverter chain as a function of supply and threshold (by body bias). Repeat d) using this analytical expression. If you observe any differences, explain where do they come from. (If it helps, you can do this part before part d)

Run each of these simulations for 5 frequency data points only.

Problem 3. Adiabatic charging.

Consider a simple RC circuit shown on the right. Assume that we want to charge the capacitor from zero volts to some final voltage V_0 . For each of the functions of V_{in} shown below, calculate the energy dissipated in the resistor. Derive the required energy expression. Assume in parts b) and c) that T is much greater than RC .

