

HOMEWORK 4.

Due: Thursday, April 8, 2003 at 5pm in 558 Cory

This is an individual assignment!

1. Conditional sum adder

- a) Find an error in a table that demonstrates conditional sum addition in slide 24, of lecture 19 notes.
- b) Demonstrate the conditional summation by a similar table for inputs $x = 10110110$ and $y = 01001101$.

2. Carry-skip adder

Read the article “Low-voltage-swing logic circuits for a 7GHz X86 integer core,” by D. Delganes et al, presented at 2004 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 154-155.

- a) Sketch the design of a 32-b carry skip adder mentioned in this paper that has a maximum of 6 pass transistors in series.
- b) Is it possible to design a 32-bit adder with only 5 pass transistors in series? If yes, please sketch that design and compare it to the design in a).

3. Ling adder

Read the article “A sub-nanosecond 0.5 μ m 64-bit adder design,” by S. Naffziger presented at 1996 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 362-363.

- a) Reconstruct the key logic equations (the equations that fully describe the operation of this adder, from the inputs to the outputs) in the design of this adder.
- b) Draw the parallel prefix tree that this adder implements.

4. Sparse Ling adder

Draw the sum-precompute gates for a sparse 64-bit Ling adder with a sparseness of 2. The final sum for both odd and even bits should be performed by selecting one of the multiple possible precomputed sums using the available carry. Use domino logic.