

HOMEWORK 5.

Due: Friday, April 23, 2004 in 558 Cory

This is an individual assignment!**1. Timing.**

A synchronous mixed-signal chip designed to work at 750MHz has the same clock source, but independent clock trees for the A/D converter (ADC) and digital baseband signal processor.

Both clock tree insertion delays are dependent on operating conditions. ADC clock insertion delay is $1.2\text{ns} \pm 0.1\text{ns}$, and the digital clock tree insertion delay is $1.5\text{ns} \pm 0.1\text{ns}$. Additionally, the local skew of both clocks is $\pm 70\text{ps}$. The ADC output register and the receiving flip-flop on the digital side are edge-triggered and have setup times of 70ps, clock-to-output delays of 150ps and 100ps hold times.

Derive the minimum and maximum logic delays for the block of combinational logic between the ADC registers and flip-flops on the digital side.

2. Timing.

For the L1-L2 latch based system from Figure 2.a. with two overlapping clocks from Figure 2.b. derive all the necessary constraints for proper operation of the logic. The latches have setup times T_{SU1} and T_{SU2} , data-to-output delays T_{D-Q1} and T_{D-Q2} , clock-to-output delays T_{CLK-Q1} and T_{CLK-Q2} , and hold times T_{H1} and T_{H2} , respectively. Relevant clock parameters are illustrated in Figure 2.b. The constraints should relate the logic delays, clock period, overlap time, T_{ov} , pulse widths $PW1$ and $PW2$ to latch parameters and skews.

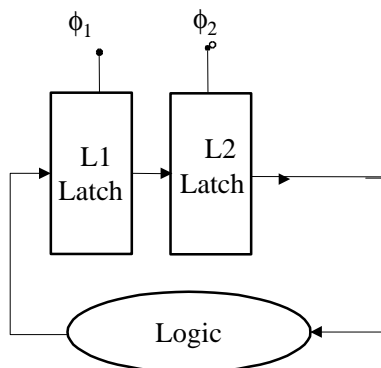


Figure 2.a

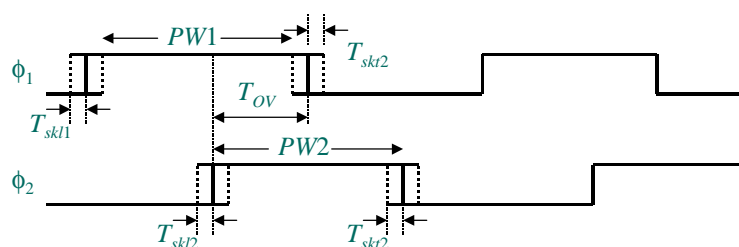


Figure 2.b