



University of California
College of Engineering
Department of Electrical Engineering
and Computer Sciences

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Thursday, May 15, 2003.

6:30-8:00pm

EE241—SPRING 2003: FINAL EXAM

NAME	Last	First
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GRAD/UNDERGRAD	
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Problem 1:

Problem 2:

Problem 3:

Total:

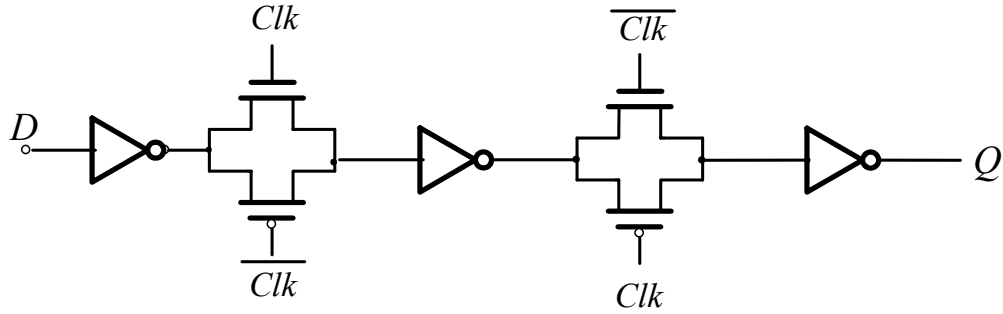
PROBLEM 1. (10 pts) MOS models, logical effort

a) (5pts) Calculate the logical effort of 3-input NAND gates and 2-input NOR gates implemented in static CMOS. Use the velocity saturated model as presented in the class:

$$I_{DSat} = \frac{W}{L} \frac{\mu_{eff} C_{ox} E_C L}{2} \frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_C L}$$

A unit inverter has a logical effort of 1. Assume 0.13 μ m technology transistors with $E_C L = 1.5V$ ($V_{DD} = 1.2V$, $V_{Th} = 0.3V$, $L = 0.13\mu m$) and step inputs.

b) (5 pts) Find the minimum achievable clock-to output delay (in terms of fanout-of-4 inverter delays) of the dynamic master slave latch pair. Ignore velocity saturation and signal slopes. Assume that the transmission gates are unit sized, with PMOS to NMOS width ratios of 2:1. Clock phases are ideal. What is the optimal $Clk-Q$ fanout of this register?



PROBLEM 2. (7 pts) Scaling.

A microprocessor implemented in 180nm technology dissipates 120W running at 1 GHz. One half of the die is occupied with 3MB of cache. You can assume that each SRAM cell has a leakage current of 10nA. You can also assume that the ratio of switching power to leakage power is 1:1 in cache and it is 9:1 in logic.

If this same processor is scaled to 130nm technology with 1.5V supply, but the amount of cache is doubled to 6MB, with leakage currents increased 3 times, what would be the power dissipation of the scaled chip running at maximum clock frequency?

PROBLEM 3. (8 pts) Logic circuits.

a) What conditions would you use for properly simulating the following cases. PMOS and NMOS transistors, supply and temperature can be either typical (T), fast (F) or slow (S). Explain your answers.

i) To check for the race conditions on the chip

ii) Worst case timing for a low voltage (e.g. $V_{DD} = 0.8\text{V}$) chip implemented in static CMOS.

iii) Worst case timing for a chip where the supply and the back biasing are controlled by the feedback loop through a DLL.

iv) Worst case supply/ground noise coupling on dynamic circuits.