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Borivoje Nikolic *Hardware Lab #1: CMOS Inverters* *EECS 141*

1. Objective

The objective of this experiment is to characterize a CMOS inverter in both loaded and unloaded conditions. By manipulating the board layout of the chip, we also hope to give further insight as to how the CMOS inverter operates.

2. Tasks

i. Wire up the CMOS inverter shown in Figure 1 and characterize it.
In order to accomplish this -

a. Obtain a 7404 inverter chip from the TA
b. Find a station w/ a breadboard, oscilloscope, and power supply and attach 5.0V to V_{dd} and ground to Gnd as shown in Figure 2.

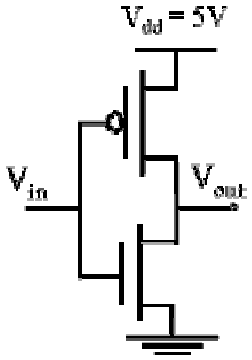


Figure 1: CMOS Inverter

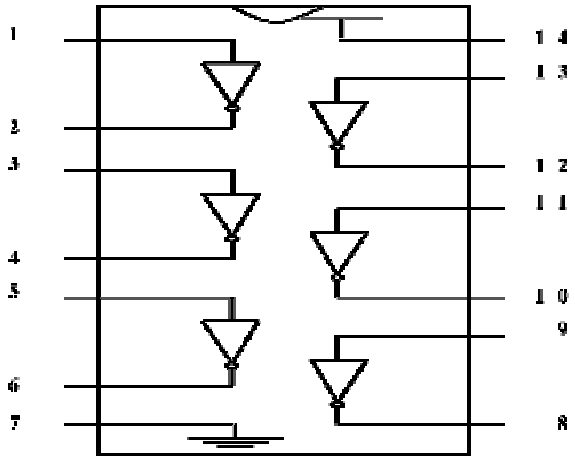
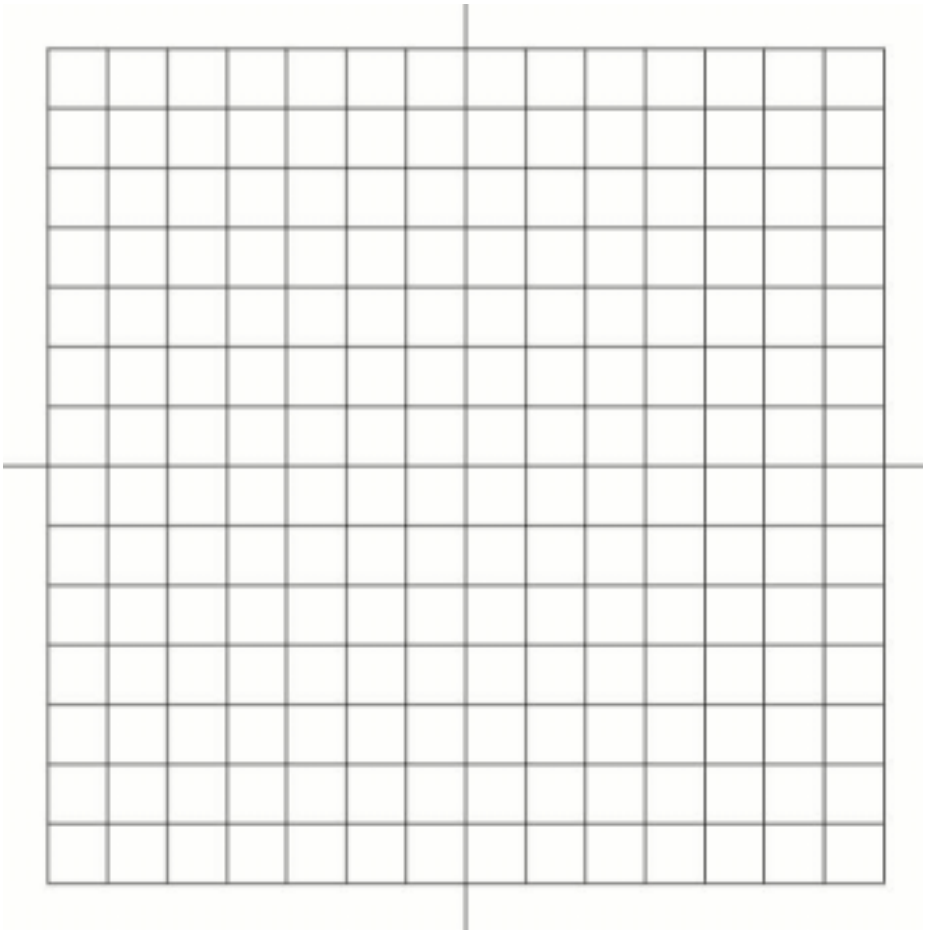


Figure 2: 7404 Inverter Chip

c. To find the VTC –
   i. Attach a 2nd variable supply to the inverter input and the 2nd Gnd to Ground.
   ii. Attach probe 1 of the scope to the inverter input, and probe 2 to the inverter output
   iii. Change the scope to XY mode by pushing **Main/Delayed** then **XY**.
   iv. Set divisions for both probes to either 1.0 or 2.0V
   v. Vary the input and display the entire VTC on the screen by hitting **AutoStore**
   vi. *Draw the image below, and estimate V_M, V_{OH}, V_{IH}, V_{OL}, and V_{IL}* – Cursors are helpful

Characterization - Experimentation	
V_M	
V_{OH}	
V_{IH}	
V_{OL}	
V_{IL}	



d. Now wire up a 10.0k resistor from Vdd to the gate output
   i. *Draw the new VTC on the same graph as above. Be sure to label the new one.*
   ii. *How does the extra resistor affect the VTC? Explain why this resistor affects it.*
   iii. *How does the resistor affect the timing characteristics (t_p, t_r, t_f)?*
   iv. *How would the VTC and timing be affected if another 10.0k resistor was added between the gate output and Gnd?*

e. To find the propagation delay –

i. Wire up a ring oscillator using 5 CMOS gates as shown in Figure 3.

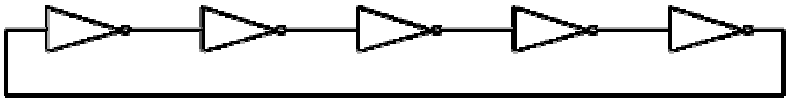


Figure 3: Ring Oscillator

ii. Using the oscilloscope, *measure its oscillation frequency at the following supply voltages* (this is easily done using **Auto Scale** and the **cursors**)
From these results, *calculate the average propagation delay per gate at each supply.*

Observed Oscillation Frequency and Calculated Average Propagation Delay t_p - Unloaded Conditions		
V_{dd}	Frequency of Oscillation	Average t_p
3.0V		
4.0V		
5.0V		
6.0V		

iii. Now attach a 50.0pF load capacitor at the output of each gate and *measure the oscillation frequency at Vdd = 5.0V*

iv. Assuming that the propagation delay is a linear function of total capacitance at the output node (a decent approximation), *calculate the approximate equivalent capacitance due to internal nodes, packaging, and wiring present at each gate output*
with no load capacitor.

Observed Oscillation Frequency and Calculated Average Propagation Delay t_p - Loaded Conditions		
Frequency of Oscillation	Average t_p	Intrinsic Capacitance

f. This part of the lab deals with power dissipation
   i. Power everything down and remove the load capacitors, leave the ring oscillator intact.
      Be sure to drive the input of the sixth inverter to Vdd.
   ii. Attach an ammeter in series between the power supply and the Vdd pin, power up, measure the average current draw from the supply. Assuming that the short circuit current is negligible, *determine the average power dissipation*.
   iii. Using the calculated power dissipation, it is now possible to determine the intrinsic load capacitance at each inverter.
      Calculate this average load capacitance, show your work.

3. Report

Please include ALL printouts, tables, and the VTC obtained from the oscilloscope.
Answer/Comment/Hand in parts italicized in Section 2.