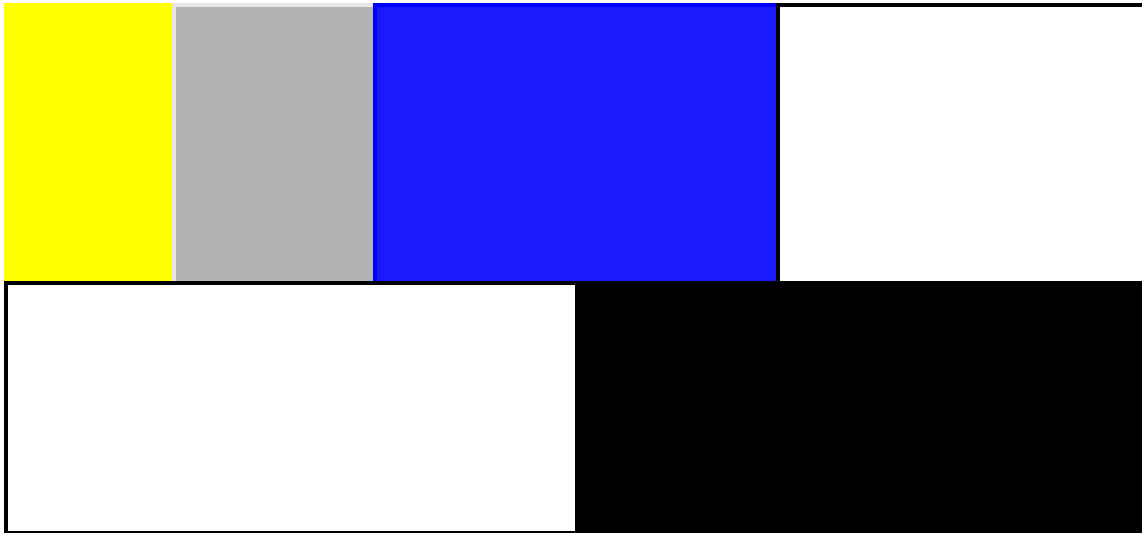


Digital Integrated Circuits - A System Perspective



SCMOS DESIGN RULES

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INSTRUCTIONS FOR DESIGNERS

DRAW IN UNITS OF LAMBDA.

**ON ANY LAYER NO SPACE OR FEATURE SIZE
MAY BE LESS THAN 2 LAMBDA WIDE.**

**FOR LAMBDA = 1.5 MICRONS, ALL
FEATURE EDGES MUST BE ON A LAMBDA GRID.
HALF LAMBDA GRID ALLOWED FOR METALS.**

**FOR LAMBDA = 1.0 MICRONS AND BELOW,
ALL FEATURE EDGES
MUST BE ON A HALF LAMBDA GRID.**

**WHAT YOU DRAW WILL BE VERY
CLOSE TO WHAT YOU GET. MOSIS
WILL TELL YOU THE DIFFERENCES.**

**SCALE YOUR CIF TO
CENTIMICRONS. NEVER SUBMIT A
DESIGN IN CENTILAMBDA.**

WHAT VALUES LAMBDA ?

LAMBDA=1.5 MICRONS
FOR 3 MICRON FABRICATORS

LAMBDA=1.0 MICRONS
FOR 2 MICRON FABRICATORS

LAMBDA=0.8 MICRONS
FOR 1.6 MICRON FABRICATORS

LAMBDA=0.6 MICRONS
FOR 1.2 MICRON FABRICATORS

TECHNOLOGIES AND REQUIRED LAYERS

PROCESS	TECHNOLOGY	REQUIRED LAYERS
PWELL AND N SUBS TWIN TUB	SCP	CWP,CSP
N WELL AND P SUBS TWIN TUB	SCN	CWN, CSN OR CSP*
ALL **	SCG	CWG,CSG
ALL ***	SCE	CWP,CWN CSP,CSN


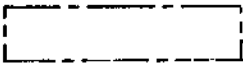








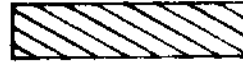




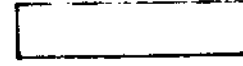
* CSP MAY ALLOW LOWER RESISTIVITY FLD POLY

** FOR A P WELL OR N SUBS TWIN TUB PROCESS,
MOSIS SETS CWP=CWG AND CSP=CSG.

FOR AN N WELL OR P SUBS TWIN TUB PROCESS,
MOSIS SETS CWN=CWG AND CSN=CSG.

*** FOR A P WELL OR N SUBS TWIN TUB PROCESS,
MOSIS IGNORES CWN AND CSN.
FOR AN N WELL OR P SUBS TWIN TUB PROCESS,
MOSIS IGNORES CWP AND USES CSP OR CSN.

LAYER NAMES AND COLORS

LAYER	CIF	CALMA #	COLOR
WELL	CWG	53	
PWELL	CWP	41	
NWELL	CWN	42	
ACTIVE	CAR	43	
SELECT	CSG	54	
PSELECT	CSP	44	
NSELECT	CSN	45	
POLY	CPG	46	
CONT TO POLY	CCP	47	
CONT TO ACT	CCA	48	
METAL1	CMF	49	
VIA	CVA	50	
METAL2	CMS	51	
CONT TO ELEC	CCE	55	
ELECTRODE	CEL	56	
OVERGLASS	COG	52	

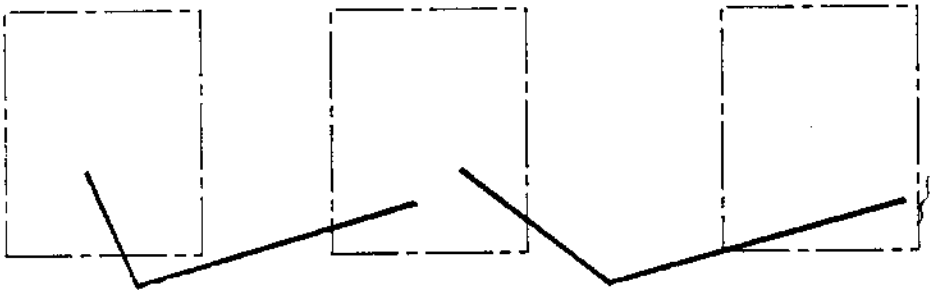
1. WELL (N WELL, P WELL)

LAMBDA S

1.1	WIDTH	10
1.2	SPACE DIFF. POT.	9
1.3	SPACE SAME POT.	0 OR 6

→ 1.1 ←

→ 1.3 ← → 1.2 ←



SAME POT.

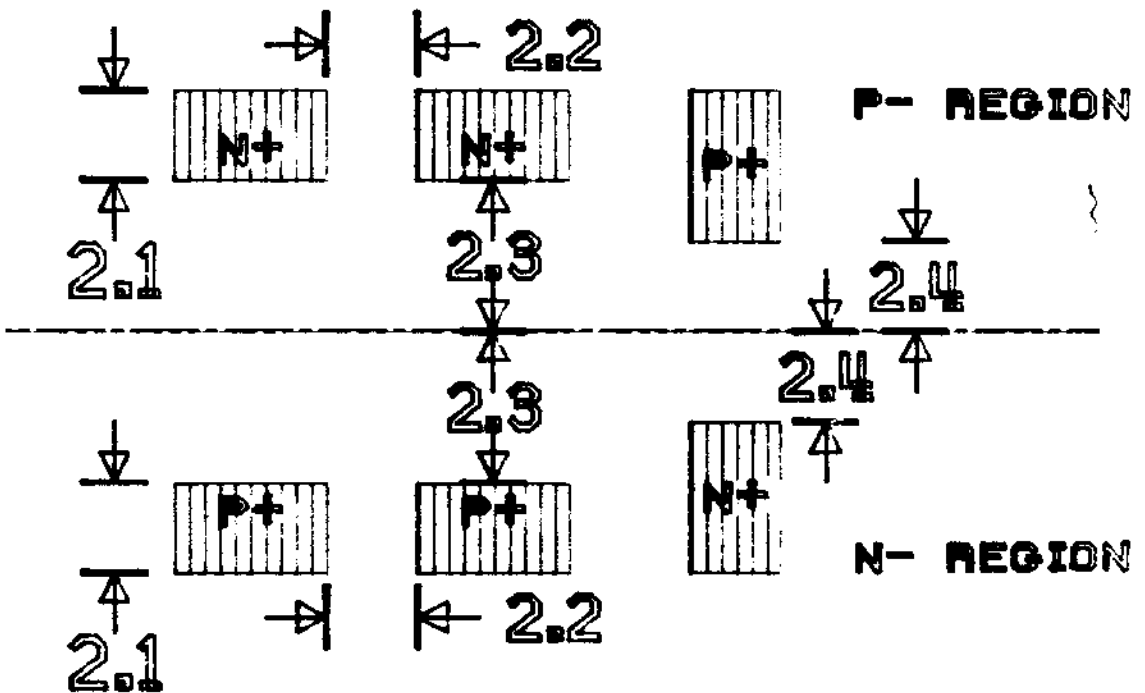
DIFF. POT.

**NOTE: IF BOTH P AND N WELLS SUBMITTED,
THEY MAY NOT OVERLAP BUT THEY MAY BE
COINCIDENT.**

2. ACTIVE

LAMBDA

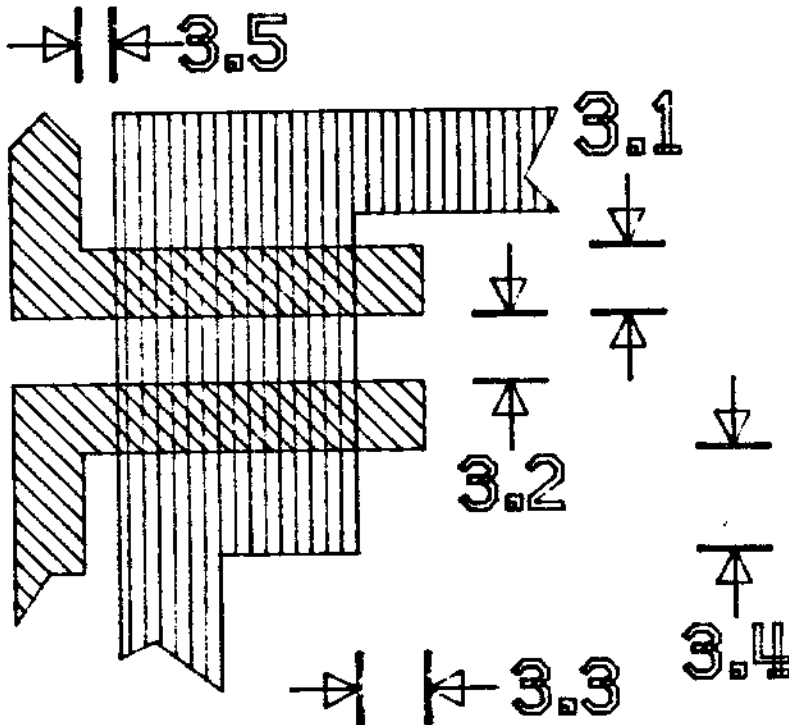
2.1	WIDTH	3
2.2	SPACE	3
2.3	SOURCE/ DRAIN ACTIVE TO WELL EDGE	5
2.4	SUBS./WELL CONTACT ACTIVE TO WELL EDGE	3



3. POLY

LAMBDA S

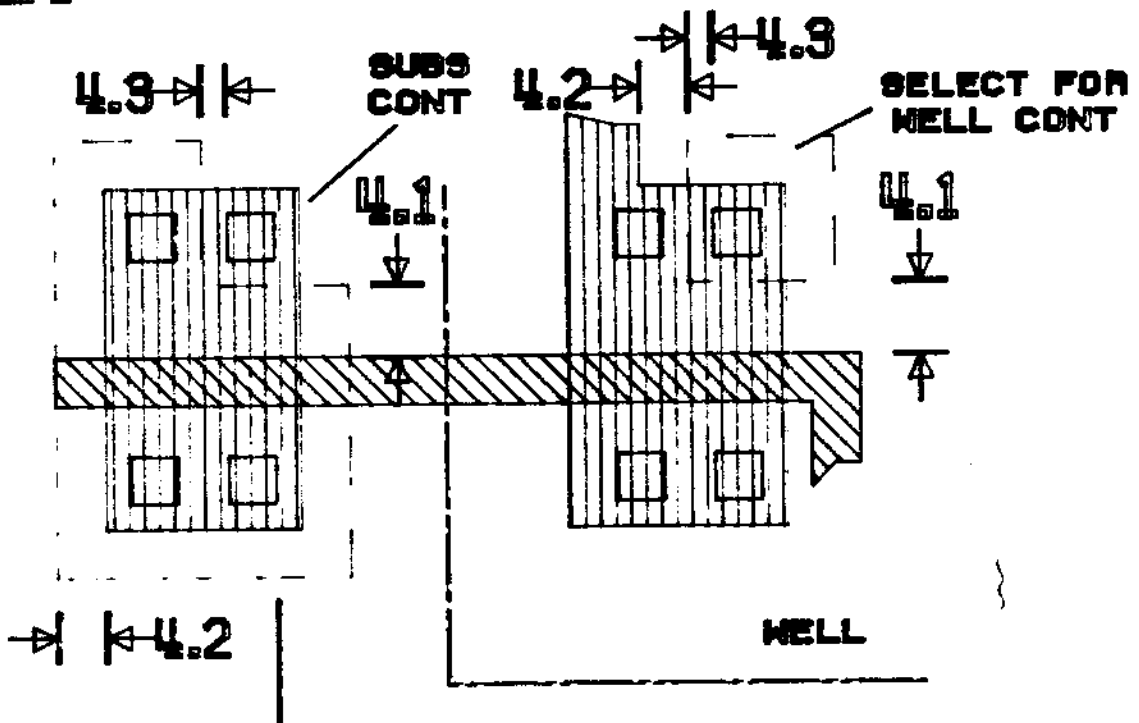
3.1	WIDTH	2
3.2	SPACE	2
3.3	GATE OVERLAP OF ACTIVE	2
3.4	ACTIVE OVERLAP OF GATE	3
3.5	FIELD POLY TO ACTIVE	1



4. SELECT (PSELECT, NSELECT)

LAMBDOAS

- | | | |
|-----|--|---|
| 4.1 | SELECT SPACE (OVERLAP)
TO (OF) CHANNEL TO ENSURE
ADEQUATE SOURCE/DRAIN WIDTH | 3 |
| 4.2 | SELECT SPACE (OVERLAP)
TO (OF) ACTIVE | 2 |
| 4.3 | SELECT SPACE (OVERLAP)
TO (OF) CONTACT TO WELL
OR SUBSTRATE | 1 |
| 4.4 | MIN WIDTH AND SPACE | 2 |



SELECT FOR XTOR

NOTE: IF BOTH PSELECT AND NSELECT
SUBMITTED, THEY MAY BE COINCIDENT
BUT MUST NOT OVERLAP

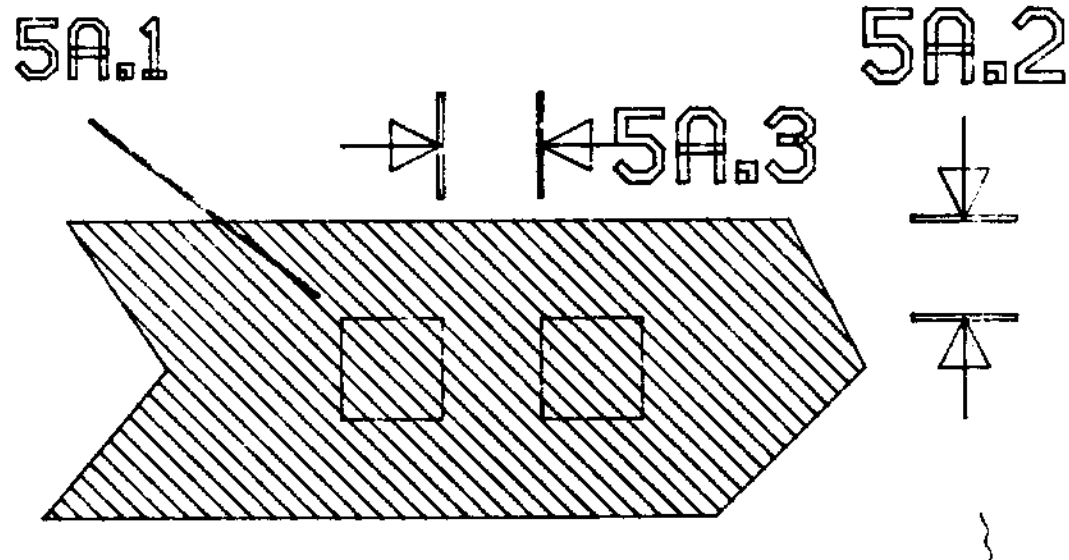
5A. SIMPLER CONTACT TO POLY

LAMBDA S

5A.1 CONTACT SIZE EXACTLY 2x2

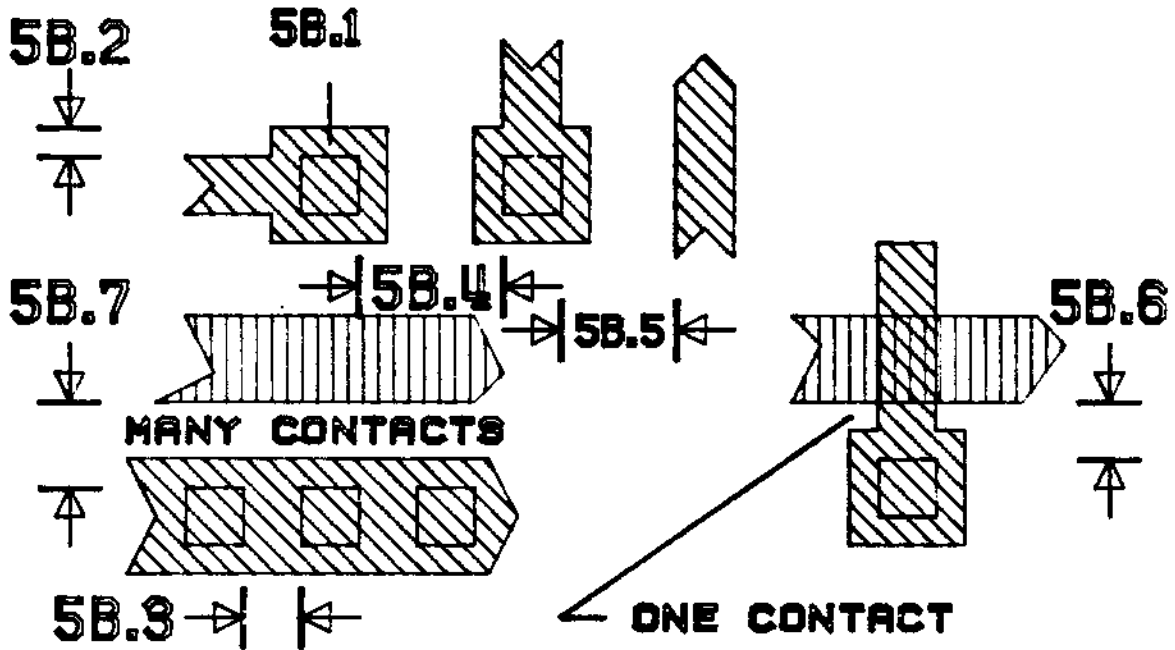
5A.2 POLY OVERLAP 2

5A.3 SPACING 2



5B. DENSER CONTACT TO POLY LAMBDRAS

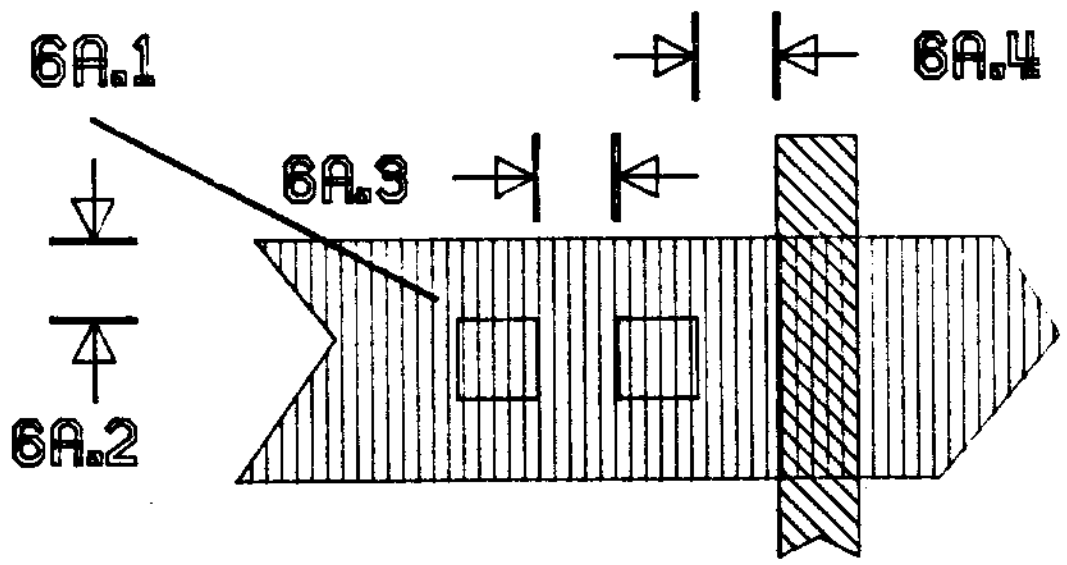
5B.1	CONTACT SIZE, EXACTLY	2x2
5B.2	POLY OVERLAP OF CONTACT	1
5B.3	SPACING ON SAME POLY	2
5B.4	SPACING ON DIFF POLY	5
5B.5	SPACE TO OTHER POLY	4
5B.6	SPACE TO ACT, ONE CONTACT	2
5B.7	SPACE TO ACT, MANY CONTACTS	3



NOTE: YOUR ASSOCIATING CONTACTS WITH POLY OR ACTIVE ALLOWS MYSIS TO INDEPENDENTLY BLOAT THE LAYER AND THE LAYER OVERLAP OF THE CONTACT

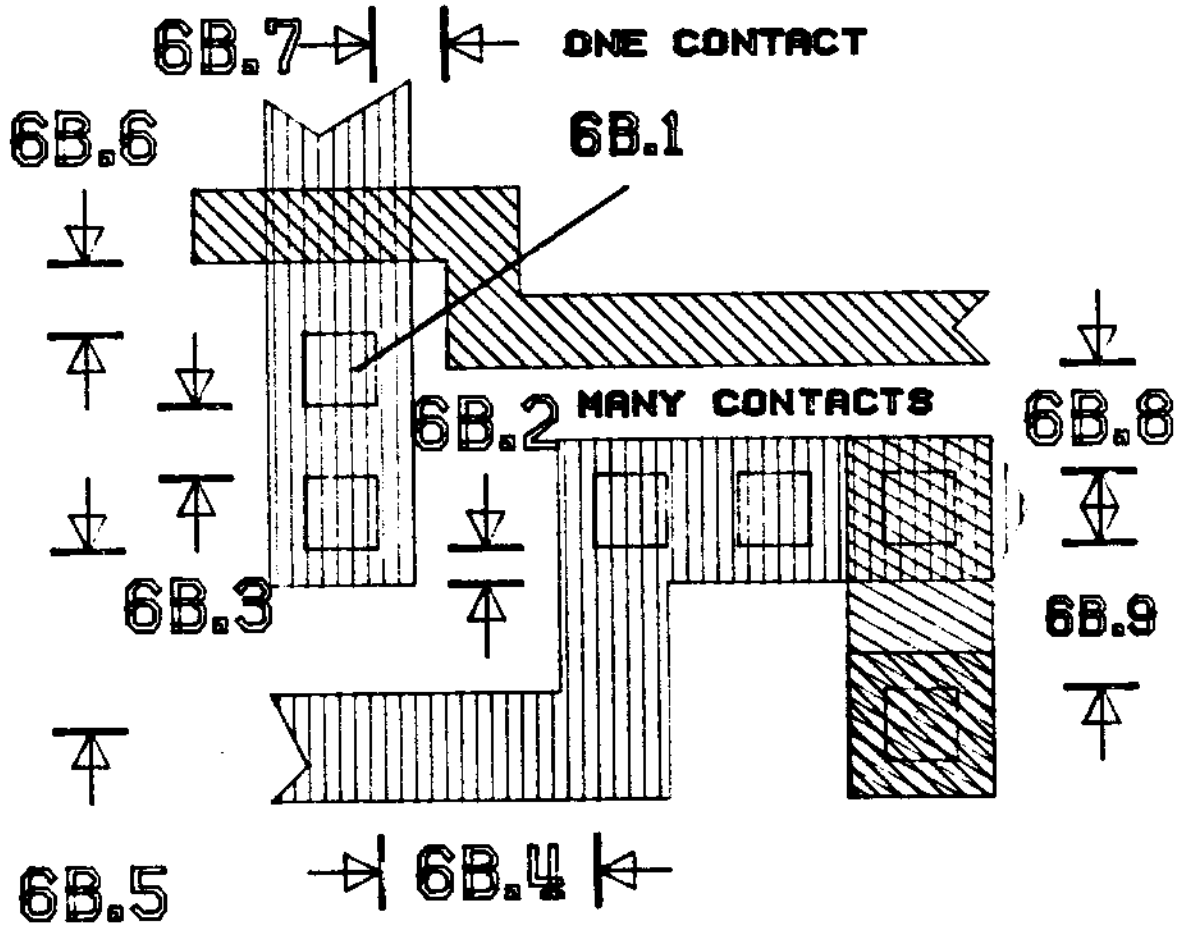
6A. SIMPLER CONTACT TO ACTIVE

		LAMBDA'S
6A.1	CONTACT SIZE EXACTLY	2x2
6A.2	ACTIVE OVERLAP	2
6A.3	SPACING	2
6A.4	SPACE TO GATE	2



6B. DENSER CONTACT TO ACTIVE LAMBDA

6B.1 CONTACT SIZE, EXACTLY	2x2
6B.2 ACTIVE OVERLAP	1
6B.3 SPACING ON SAME ACTIVE	2
6B.4 SPACING ON DIFF ACTIVE	6
6B.5 SPACE TO DIFF ACTIVE	5
6B.6 SPACE TO GATE	2
6B.7 SPACE TO FIELD POLY. ONE CONT.	2
6B.8 SPACE TO FIELD POLY. MANY CONT.	3
6B.9 SPACE TO CONTACT TO POLY	4



7. METAL1

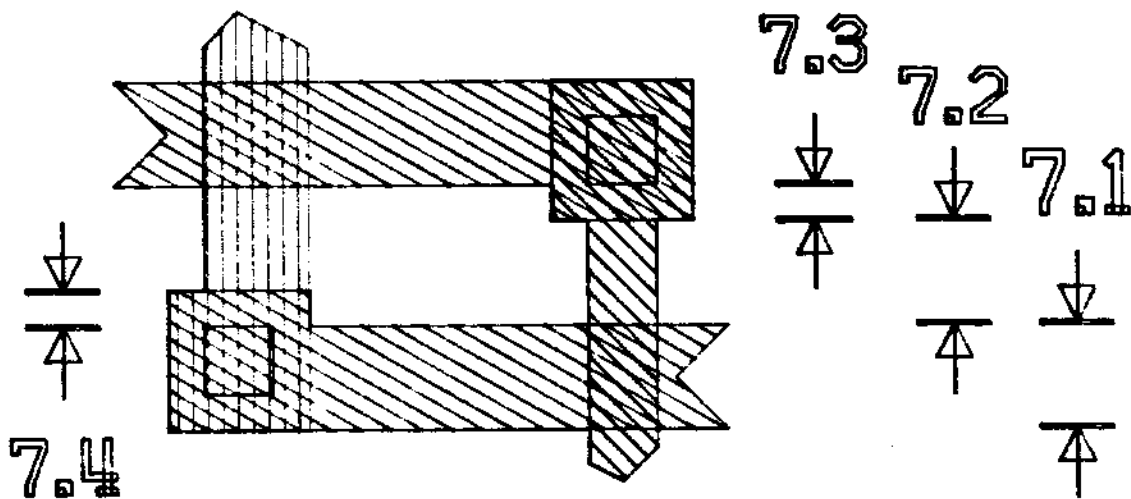
LAMBDA5

7.1 WIDTH 3

7.2 SPACE TO METAL1 3

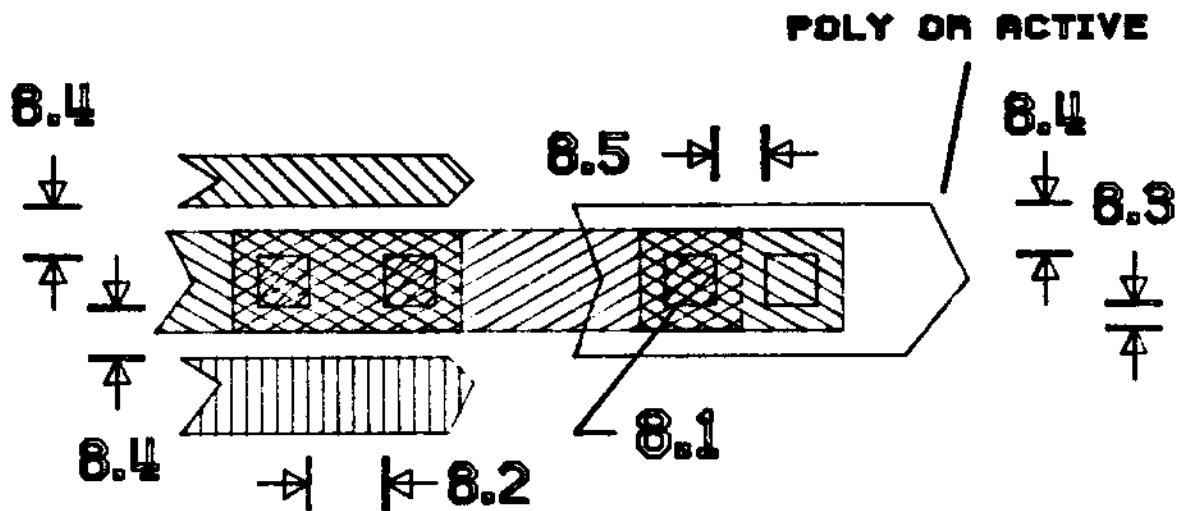
7.3 OVERLAP OF CONTACT TO POLY 1

7.4 OVERLAP OF CONTACT TO ACTIVE 1



8. VIA

	LAMBDA'S
8.1 SIZE, EXACTLY	2x2
8.2 SEPARATION TO VIA	3
8.3 OVERLAP BY METAL1	1
8.4 SPACE TO POLY OR ACTIVE EDGE	2
8.5 SPACE TO CONTACT	2



NOTE: OBJECTIVE IS VIA ON A FLAT SURFACE. VIA STACKED OVER CONTACT NOT ALLOWED.

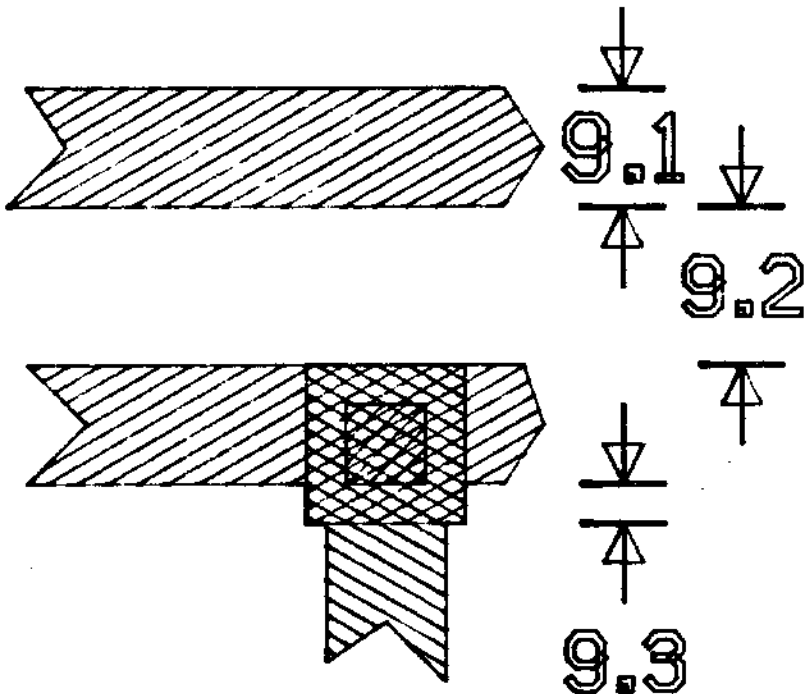
9. METAL2

LAMBDA8

9.1 WIDTH 3

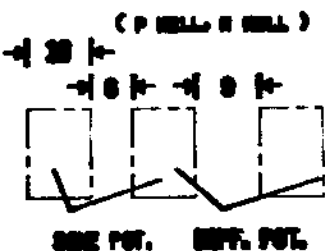
9.2 SPACE TO METAL2 4

9.3 OVERLAP OF VIA 1

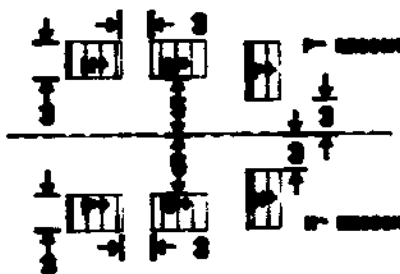


MOSIS CMOS SCALABLE RULES (REV6)

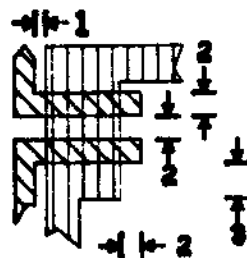
WELL



ACTIVE

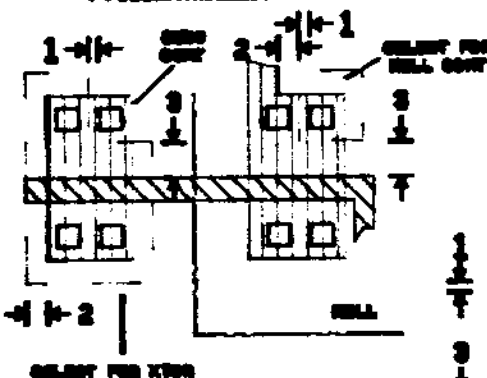


POLY

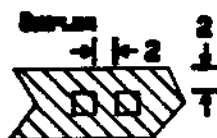


SELECT

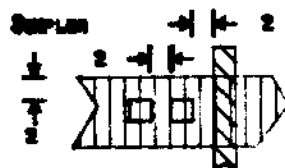
(PSELECT & NSELECT)



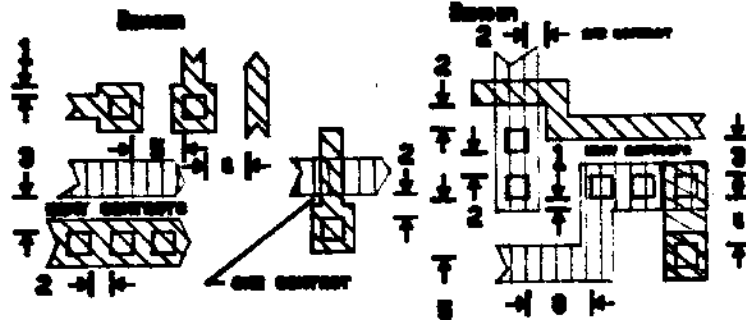
CONTACT TO POLY



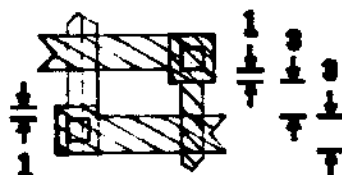
CONTACT TO ACTIVE



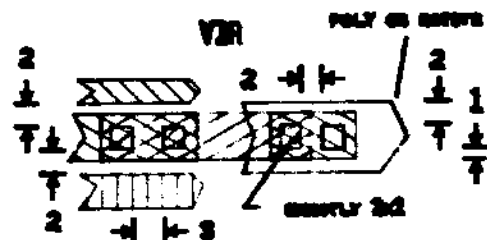
OVERLAP SPECIFICALLY 2x2



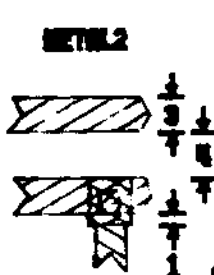
METAL1



VIA



METAL2



OVERGLASS



FRAME FOR TESTS AND
BONDING FOR PACKING ARE
MET2 UNDER OTHER OVERGLASS

LAYER	CF	COIN	COLOR
WELL	CGG	53	
PWELL	CHP	41	
NWELL	CHN	42	
ACTIVE	CHA	43	
SELECT	CSG	51	
PSELECT	CHP	41	
NSELECT	CHN	42	
POLY	CPG	46	
CONT TO POLY	CCP	47	
CONT TO ACT	CCA	48	
METAL1	CHF	49	
VIA	CHV	50	
METAL2	CHS	51	
CONT TO ELEC	CCE	55	
ELECTRODE	CEL	56	
OVERGLASS	COG	52	

ALL LAYERS MUST BE ON LOWER SIDE EXCEPT
METALS WHICH CAN BE ON BOTH SIDES