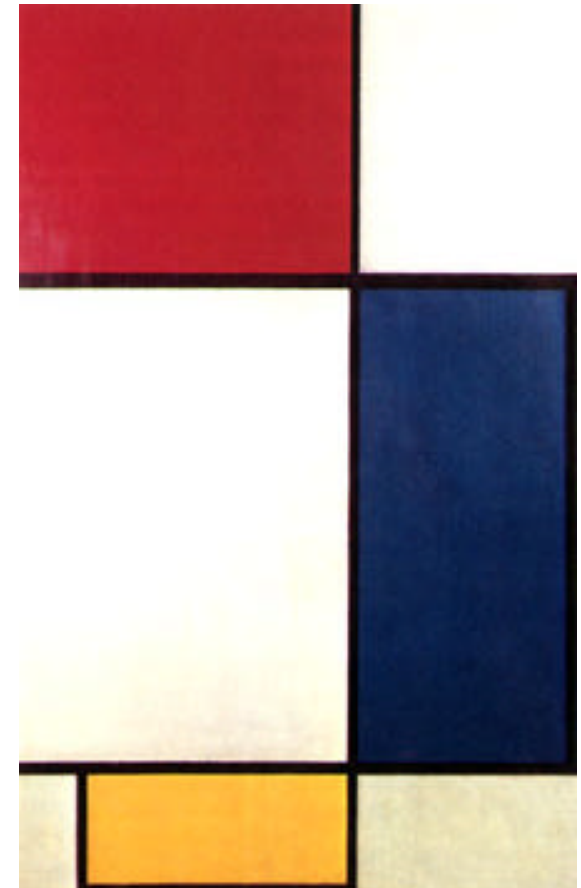
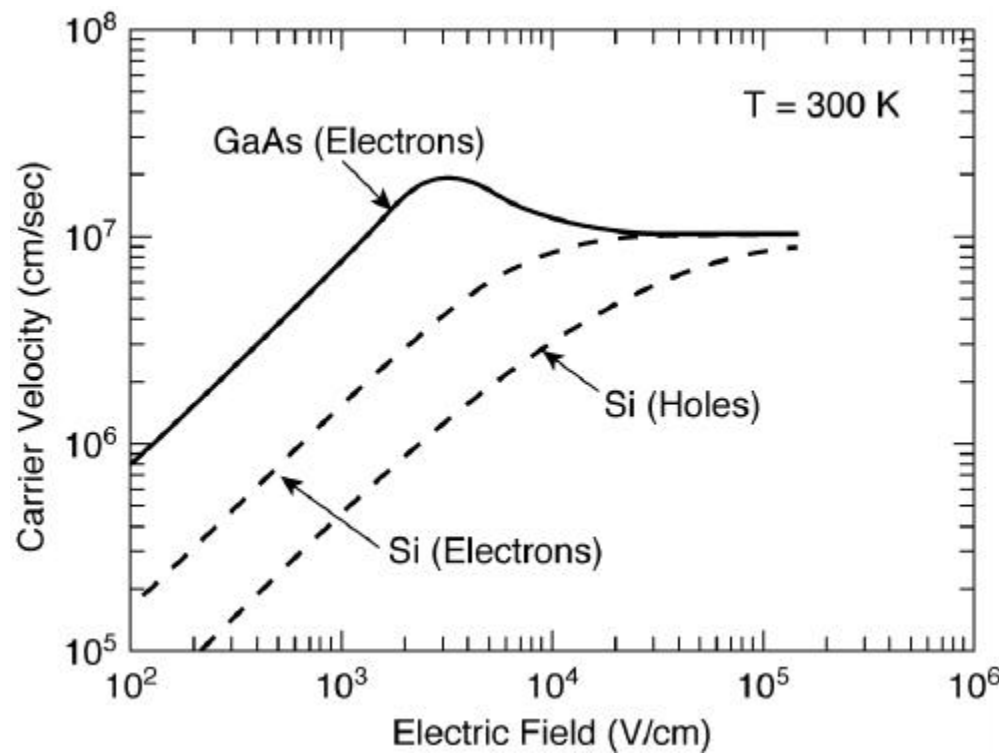

VERY HIGH PERFORMANCE LOGIC



Note

**Slides on High-Speed Bipolar
and Superconduction not yet
available**

GaAs Design



Increased Mobility at Low Electrical Field

Higher Performance

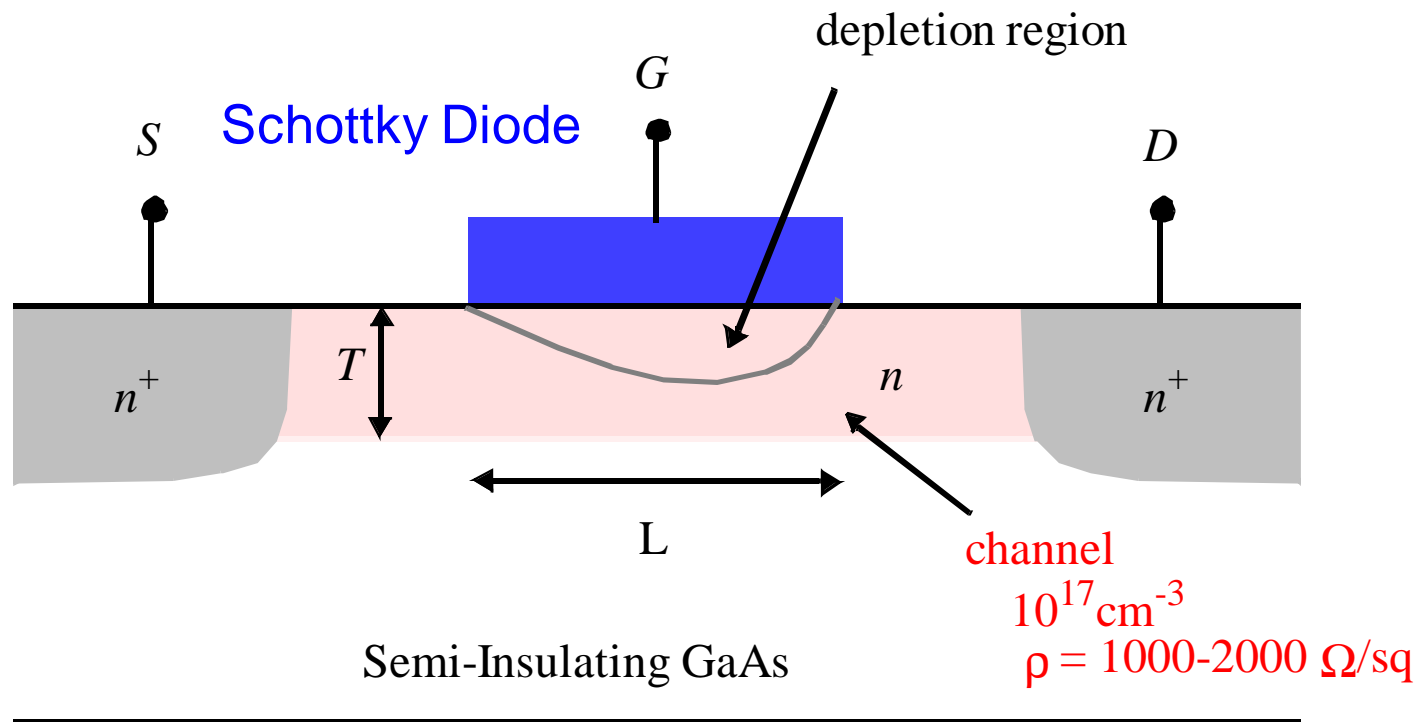
GaAs Material Properties

- Max electron velocity = 2 x Silicon = 2×10^7 cm/sec
- Hole mobility GaAs (= 400) < Si (489 cm²V/sec)
Excludes complementary logic
- Electron mobility GaAs (4000-9000) >> Si (500-1200)
- Maximum Field (max velocity) GaAs (0.3 V/μm) < Si (1 V/μm)
Should operate at low voltages
- Schottky Barrier Height GaAs (0.6-0.8V) > Si (0.4-0.6 V)
- Bandgap Energy GaAs (1.43 eV) > Si (1.11 eV)
Radiation hard
- Resistivity GaAs ($1 \cdot 10^9 \Omega/\text{sq}$) >> Si ($1 \cdot 10^5 \Omega/\text{sq}$)
Semi-insulating

GaAs Material Problems

- Brittle Material \Rightarrow 3 to 4 inch wafers
- High Defect Density
 Low Yield (100 to 1000 times smaller vs. Si)
- Q_{SS} and Q_{ox} large
 NO MOS transistors!
- Hole mobility low
 No complementary gates

Favored Device: MESFET



MESFET Operation

if($V_G == 0$): transistor ON — part of channel depleted

if ($V_G \uparrow$): depletion layer $\downarrow \Rightarrow$ conductivity \uparrow

if ($V_G \downarrow$): depletion layer $\uparrow \Rightarrow$ conductivity \downarrow

if ($V_G == V_P$): pinchoff, no conductance

DEPLETION TRANSISTOR

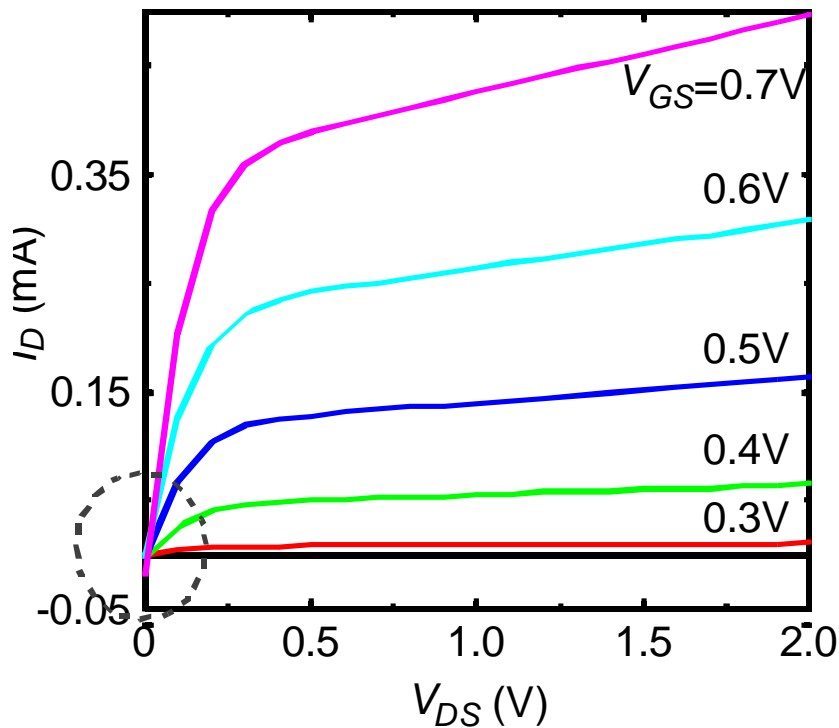
Enhancement transistors also available

V_P (enhancement): 0 V — 0.2 V

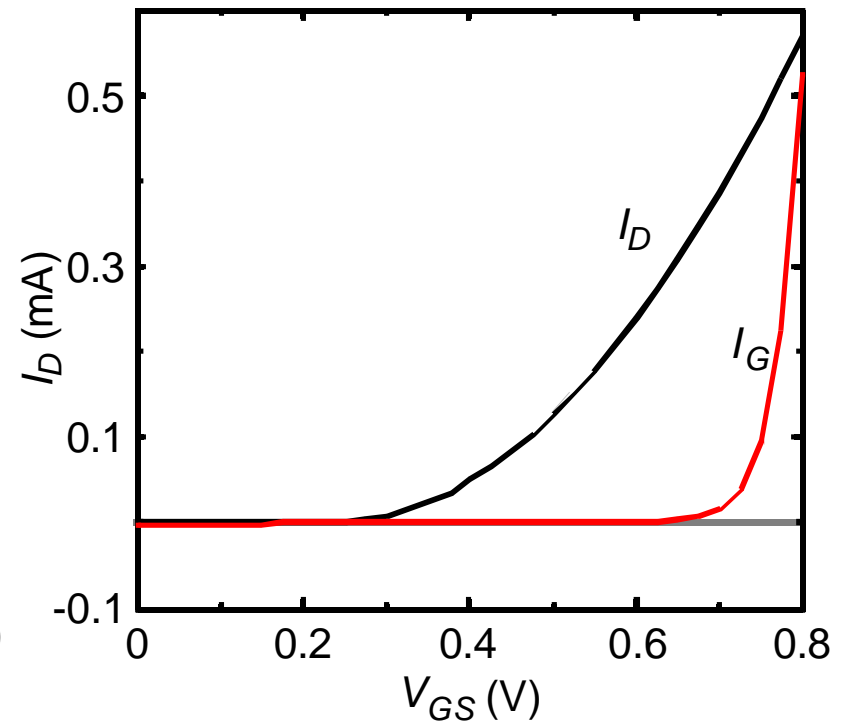
V_P (depletion): -0.7 V — -2 V

Large variations of V_P over die (100 — 200 mV)!

I-V Characteristic



(a) I_D - V_{DS} characteristic



(b) I_D - V_{GS} characteristic ($V_{DS} = 0.5$ V)
 I_G is the current flowing into the gate.

Curtice Model

Drain Current:

$$I_D = \begin{cases} 0 & \text{for } (V_{GS} < V_P) \\ \beta(V_{GS} - V_P)^2(1 + \lambda V_{DS}) \tanh(\alpha V_{DS}) & \text{for } (V_{GS} > V_P) \end{cases}$$

Gate Current:

$$I_G = I_S \left(e^{V_G / n \phi_T} - 1 \right)$$

	β (A/V ²)	V_{P0} (V)	λ (1/V)	α (1/V)	I_S (A)	n
Enhancement	250×10^{-6}	0.23	0.2	6.5	0.5×10^{-3}	1.16
Depletion	190×10^{-6}	-0.825	0.0625	3.5	10^{-2}	1.18

Parameters for 1 mm GaAs Process

GaAs MESFET Model

.model enh njf

*+ vto=0.23 beta=250u lambda=0.2 alpha=6.5 ucrit=0 gamds=0
ldel=-0.4u wdel=-0.15u*

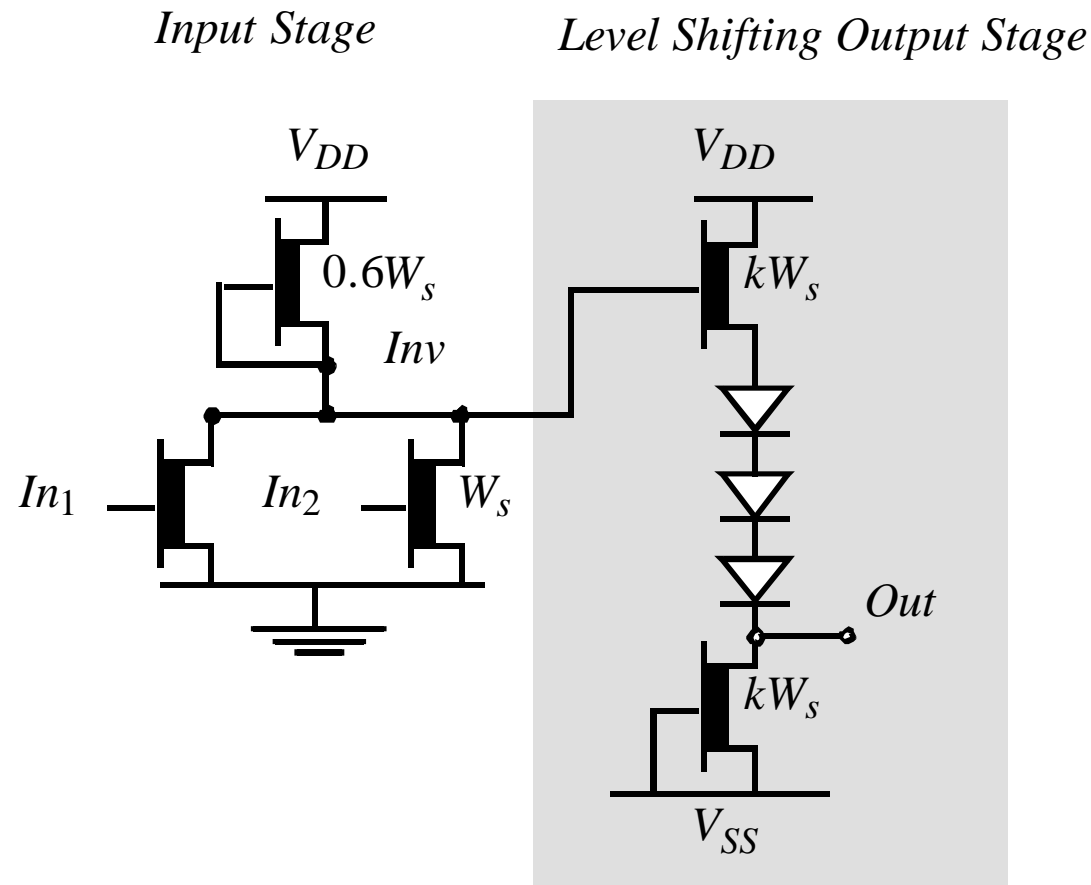
+ rsh=210 n=1.16 is=0.5m level=3 sat=0 acm=1 capop=1

.model dp njf

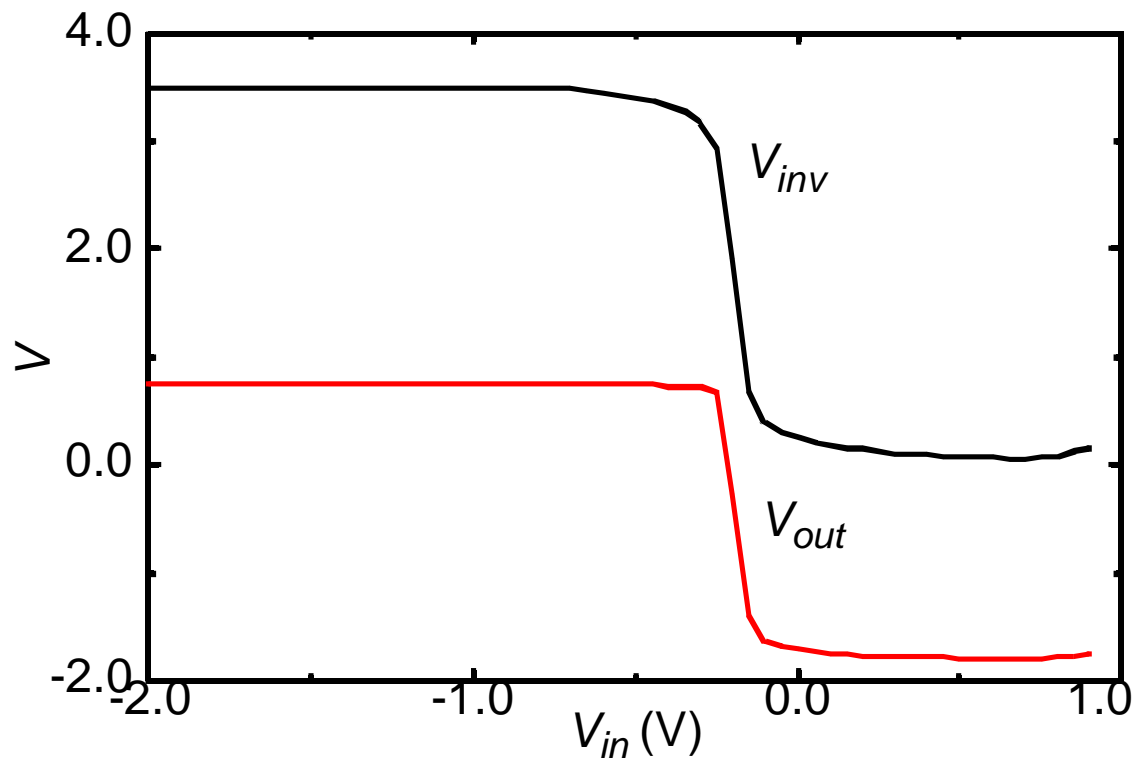
*+ vto=-0.825 beta=190u lambda=0.065 alpha=3.5 ucrit=0 gamds=0
ldel=-0.4u wdel=-0.15u*

+ rsh=210 n=1.18 is=10m level=3 sat=0 acm=1 capop=1

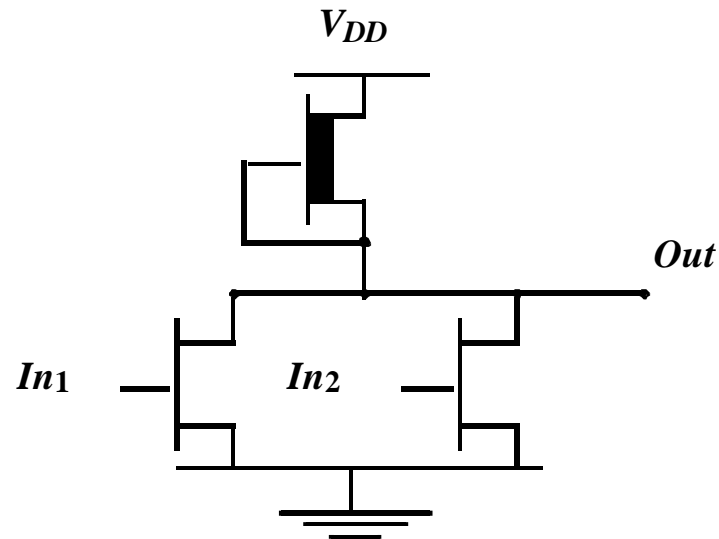
Buffered FET Logic (BFL)



Voltage Transfer Characteristic



Direct-Coupled Fet Logic (DCFL)



Max Input Voltage : +/- 0.7 V

Strict Control of Threshold Voltage Required (+/- 0.1 V)

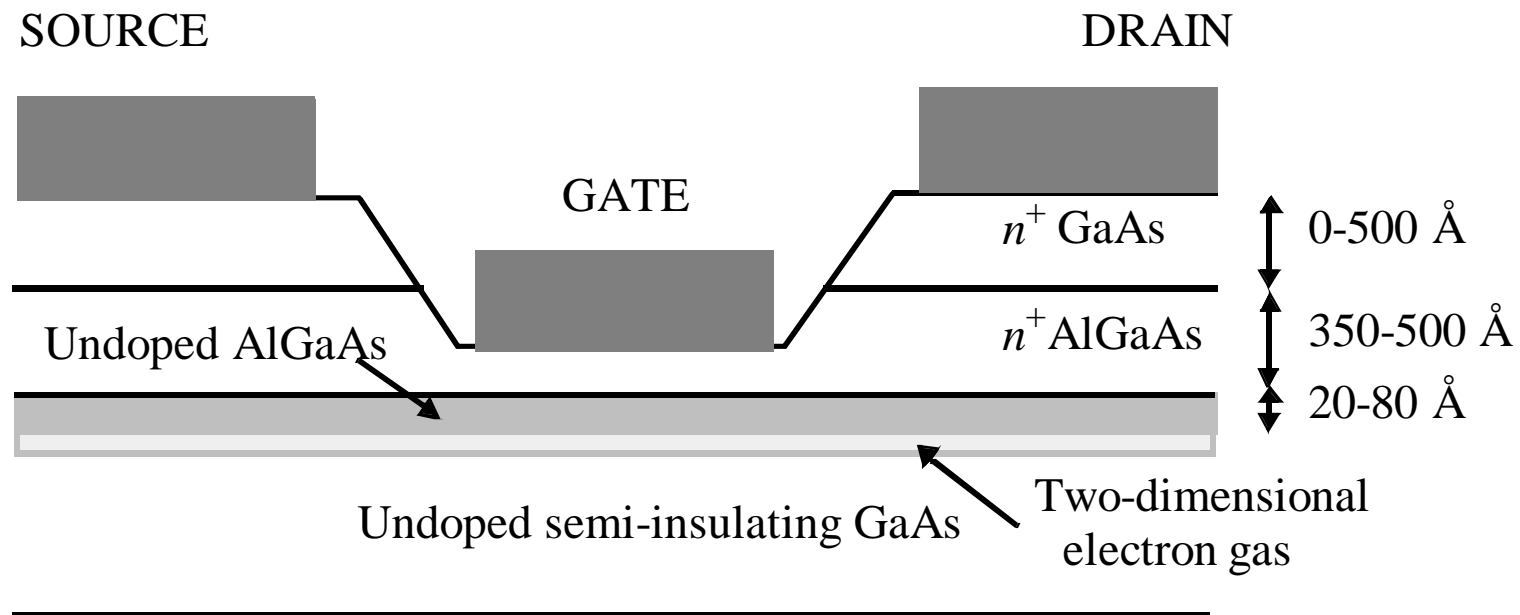
Asymmetrical Response

Sensitive to Fanout

Logic Families - Comparison

Logic Family	t_{p0} (psec)	$\Delta t_p/FO$ (psec/FO)	t_p/C_L (psec/ fF)	P (mW/ gate)
BFL (1 μm)	90	20	0.67	10
BFL (0.5 μm)	54	12	0.67	10
DCFL (1 μm)	54	35	1.84	0.25
SCFL	BFL range	low	low	~5
DCFL HEMT (0.5 μm - 77°K)	11	7	0.32	1.3

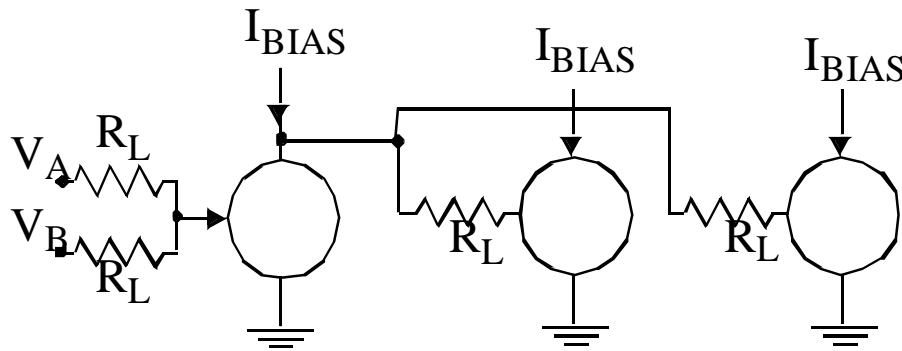
High Electron Mobility Transistor (HEMT)



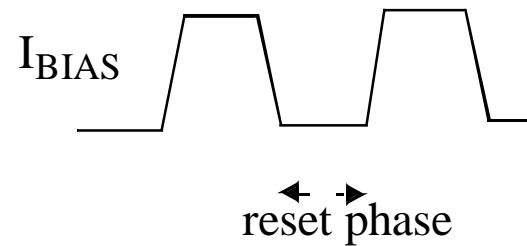
Mobility in Undoped GaAs $> 8500 \text{ cm}^2/\text{Vsec}$ ($4500 \text{ cm}^2/\text{Vsec}$ in Doped GaAs)

Up to $50,000 \text{ cm}^2/\text{Vsec}$ at Liquid Nitrogen Temperature

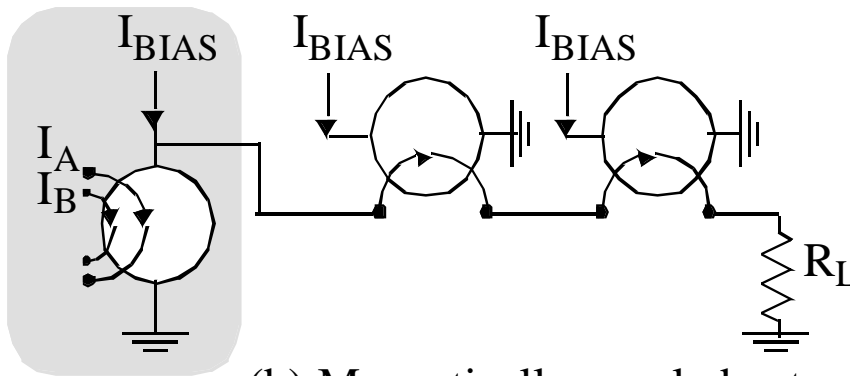
JJ Logic Families



(a) Current injection gate

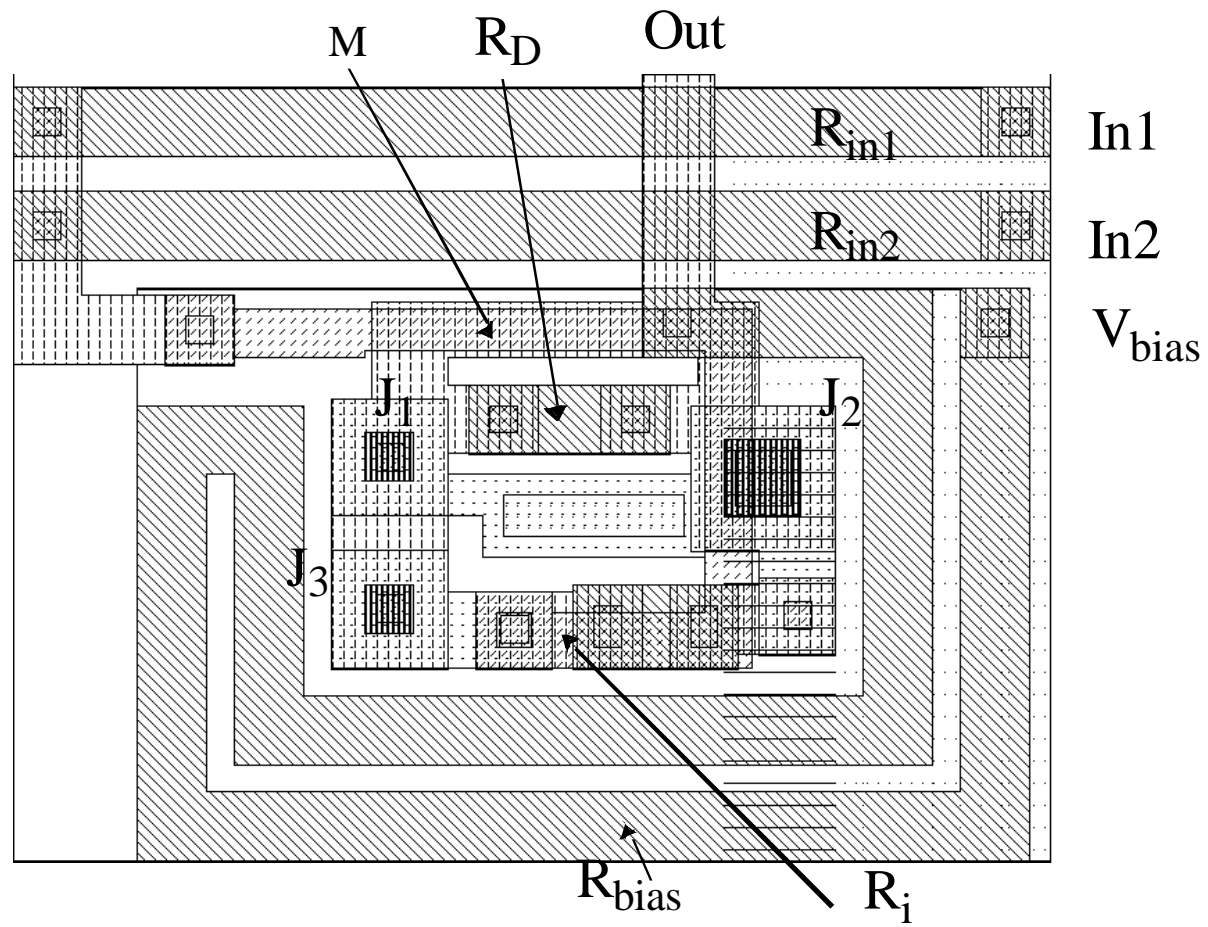


(c) bias current waveform



(b) Magnetically coupled gate

MVTL Gate Layout



MVTL Transient Response

