



**University of California at Berkeley**  
**Department of Electrical Engineering and Computer Science**

**EECS 141: First Midterm Exam, Fall '96**

**Renu Mehra**

**26th Sept. 1996**

Please PRINT your name and sign below. Also, write your name in each sheet before you start. Use the space provided to answer all questions. You can use the back side of the sheet if needed. Show your work for full credit.

Name: \_\_\_\_\_  
(last) (first)

Signature: \_\_\_\_\_

**Transistor parameters:**

|              | NMOS                        | PMOS                        |
|--------------|-----------------------------|-----------------------------|
| $V_{T0}$     | 0.7                         | -0.7                        |
| $k'_n, k'_p$ | $20 \mu\text{A}/\text{V}^2$ | $60 \mu\text{A}/\text{V}^2$ |
| $L_d$        | $0 \mu\text{m}$             | $0 \mu\text{m}$             |

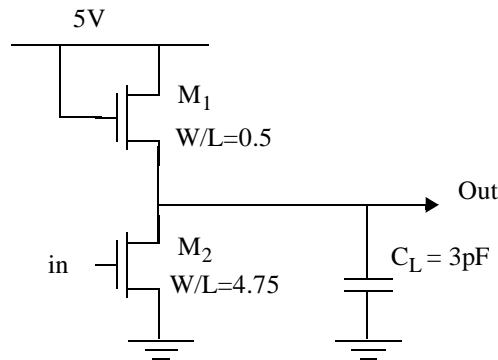
Neglect body effect and channel-length modulation.

**Grades**

|            |  |
|------------|--|
| Problem #1 |  |
| Problem #2 |  |
| Total      |  |

**Name:** \_\_\_\_\_

**Problem 1.** Bill needs to implement an inverter in an NMOS only process. He decides to use a saturated enhancement mode load as shown in the figure below. The total load capacitance on the inverter is 3pF.



1(a) Find the  $V_{OL}$  of the above circuit.

$V_{OL}$ : \_\_\_\_\_

1(b) Bill finds out that the NMOS process he is using has a variation of  $\pm 0.5V$  in the threshold voltages ( $V_T$ ) of its devices and that devices in the same chip can have different thresholds. What threshold voltages of  $M_1$  and  $M_2$  will give the highest  $V_{OL}$ ?

$V_{T1}$ : \_\_\_\_\_  $V_{T2}$ : \_\_\_\_\_

Name:

1(c) Find the  $V_{OL}$  of the inverter with threshold voltages computed in part (b).

$V_{OL}$ :

1(d) Explain qualitatively how the following properties of the inverter are affected as the threshold voltages change from part (a) to part (b). If you are unsure of your  $V_{OL}$  values, assume that it increases by 0.1V from part (a) to part (c). Identify what changes in the different parameters led to your conclusions.

|                           | Increase/<br>Decrease? | Why? |
|---------------------------|------------------------|------|
| Static power dissipation  |                        |      |
| Dynamic power dissipation |                        |      |

Name:

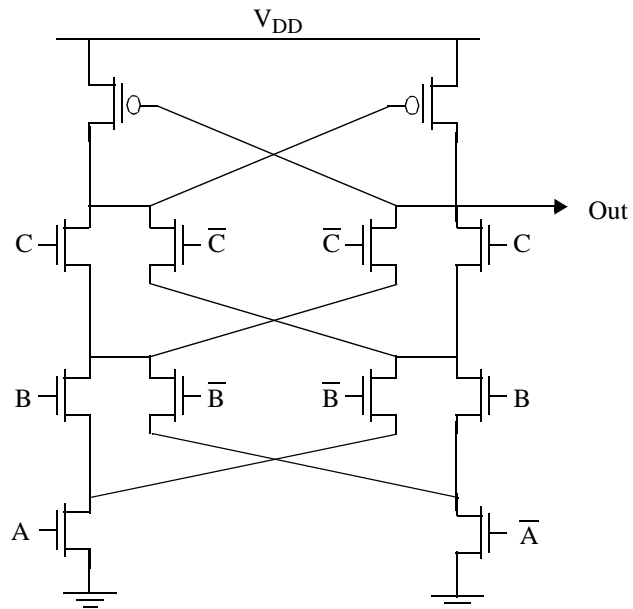
|           | Increase/<br>Decrease? | Why? |
|-----------|------------------------|------|
| $t_{pHL}$ |                        |      |

1(e) In an attempt to reduce improve  $V_{OL}$ , Bill decides to double the size of the NMOS pull-down transistor. Explain qualitatively how his decision affects the following properties and identify what changes in the different parameters led to your conclusions. The threshold voltages are the same as in part (a).

|                           | Increase/<br>Decrease? | Why? |
|---------------------------|------------------------|------|
| Static power dissipation  |                        |      |
| Dynamic power dissipation |                        |      |
| $t_{pHL}$                 |                        |      |

**Name:**

**Problem 2.**



2(a) Determine the logic function of the above circuit. Identify the function.

Out =

2(b) Does the size of the PMOS transistor affect the functionality of the circuit? Briefly explain why or why not?

**Name:**

2(c) What is the static power consumption of the circuit?

2(d) Derive the pull-up and pull-down networks to implement the above logic in complementary CMOS logic style. You can assume that both the inputs and their complements are available. Use 10 transistors or less in each of the pull-up and pull-down networks.

Name:

- 2(e) Find W/L ratios of the devices in your network so that the  $t_{pLH}$  and  $t_{pHL}$  of your gate are the same as that of a CMOS NAND gate with  $W/L = 2$  for both the NMOS and PMOS transistors.