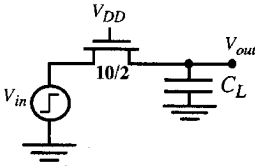


Problem 1: Static and dynamic analysis

Total: 15

Consider the following logic circuit:



- a. Assume that $V_{out}(t=0) = 0$ V. Determine $V_{out}(t=\infty)$ when V_{in} is raised from 0 V to V_{DD} at $t=0$. Assume $V_{DD} = 3$ V. You may assume that $L = L_{eff}$, or that the lateral diffusion can be ignored in this problem.

$$V_{out}(t=\infty) = V_{DD} - V_T(V_{out})$$

$$= 3 - (0.7 + 0.5(\sqrt{V_{GS} + V_{out}} - \sqrt{V_{GS}}))$$

Iterate for solution

$V_{out}(t=\infty):$ 1.89V
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- b. Determine t_{pLH} at V_{out} . Assume an ideal step at the input. The external load capacitance C_L can be assumed to be large and equals 10 pF.

$$V_{swing} = 1.89\text{V} \rightarrow V_{50\%} = 0.95$$

Transistor always in saturation!

$$I(V_{out}=0) = \frac{1}{2} \cdot \frac{10}{2} \cdot 20 (3 - 0.75)^2 = 253 \mu\text{A}$$

$$I(V_{out}=0.95) = \frac{1}{2} \cdot 5 \cdot 20 (3 - 0.95 - V_T')^2 = 61.6 \mu\text{A}$$

$$V_T'(V_{out}=0.95) = 0.94\text{V}$$

$$I_{av} = (253 + 61.6) / 2 = 157.3 \mu\text{A}$$

$$t_{pLH} = \frac{10 \text{ pF} \times 0.95}{157.3 \mu\text{A}}$$

$t_{pLH} = 60 \text{ nsec}$

c. Determine the energy that is stored on C_L at the end of the low-to-high transition. How much energy was dissipated in the MOS transistor? How much was delivered by the input source? HINT: Derive the results; Do not take the equations in the book for granted!

$$E_{CL} = \frac{C_L V_{sw}^2}{2} = \frac{10\text{pF} \cdot 1.89^2}{2} = 17.9 \text{ pJ}$$

$$E_{vin} = C_L V_{sw} V_{dd} = 10 \times 1.89 \times 3 = 56.7 \text{ pJ}$$

$$E_{nos} = E_{vin} - E_{CL} = 38.3 \text{ pJ}$$

$E(C_L) =$	17.9 pJ
$E(MOS) =$	38.3 pJ
$E(V_{in}) =$	56.7 pJ

d. Assume that the NMOS is replaced by a PMOS device of the same size with its gate connected to GND. Determine the impact on the following design parameters, and give a short explanation

EXPLAIN:

$V_{out}(t = \infty):$ <input checked="" type="checkbox"/> Larger <input type="checkbox"/> Equal <input type="checkbox"/> Smaller	PMOS charges all the way to $V_{DD} \rightarrow V_{out}(\infty) = 3V$
$t_{pLH}:$ <input checked="" type="checkbox"/> Larger <input type="checkbox"/> Equal <input type="checkbox"/> Smaller	There is more current drive for PMOS (no body effect), get PMOS has larger transconductance \rightarrow overall slower
$E(V_{in}):$ <input checked="" type="checkbox"/> Larger <input type="checkbox"/> Equal <input type="checkbox"/> Smaller	Higher swing at the output

e. Describe in a couple of sentences how you would decrease the delay of this gate. Is there an absolute lower limit on the delay, and if yes explain why and give an approximate value of this delay.:

How would you reduce the delay?

Make transistor larger: $(\frac{W}{L})_{NMOS} \uparrow$

3

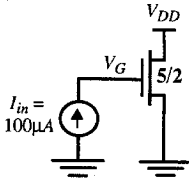
Absolute minimum delay? Why?

At some point, intrinsic capacitance of NMOS becomes dominant $> 10\text{pF}$ \rightarrow delay remains constant

Approximate value of minimum delay

The minimum delay is approximately equal to the delay of an unloaded minimum size inverter (t_{p0})

PROBLEM 2: MOS Capacitances



Consider the following simple circuit (implemented in the $1.2 \mu\text{m}$ CMOS technology). Assume $V_{DD} = 3 \text{ V}$ and use the following transistor parameters: $C_{ox} = 1.75 \text{ fF}/\mu\text{m}^2$, x_j (lateral diffusion) = $0.15 \mu\text{m}$, $C_{j0} = 3.0 \times 10^{-4} \text{ F}/\text{m}^2$, $m_j = 0.5$, $C_{jsw} = 8.0 \times 10^{-10} \text{ F}/\text{m}$, $m_{jsw} = 0.5$.

Assume that V_G is initially at 0 V . We want to compute the time it will take to raise V_G to V_{DD} . To do so, we will lump the device parasitic capacitances into a single lumped capacitance. This capacitance is a function of the operation region of the device.

a. Determine the operation regions the MOS transistor is traversing during the transient (for V_G going from 0 to V_{DD}).

Region 1:

cutoff $V_G < V_T$

Region 2:

saturation $V_T < V_G < V_{DD}$

Region 3:

...

b. Determine the (average) lumped capacitance seen at the gate of the MOS transistor in each of these regions.

4

cutoff: $C_g = C_{ox} \cdot W \cdot L = 1.75 \times 3 \times 1.2 = 6.3 \text{ fF}$

4

saturation: $C_g = \underbrace{C_{ox} \cdot W \cdot L}_{\text{overlap}} \cdot 2 + \frac{2}{3} C_{ox} \cdot W \cdot L_{\text{left}}$

$$= 1.75 \cdot 3 \cdot 0.3 + \frac{2}{3} \cdot 1.75 \cdot 3 \cdot 0.9$$

$$= 4.725 \text{ fF}$$

C_g (region 1):

6.3 fF

C_g (region 2):

4.725 fF

C_v (region 3):

—

c Determine the total time it will take for V_G to go from 0 V to V_{DD} (for $I_{in} = 100 \mu\text{A}$),

$$t_1 = \frac{\Delta V \cdot C_G}{I} = \frac{0.75 \cdot 6.3 \text{ pF}}{100 \text{ nA}} = 47 \text{ ps}$$

$$t_2 = \frac{(3 - 0.75) \cdot 4.725 \text{ pF}}{100 \text{ nA}} = 106.3 \text{ ps}$$

$$t_{tot} = t_1 + t_2$$

$t(0 \rightarrow V_{DD})$:

153 ps