

# EE241 S06 Homework #1

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The goal of this assignment is to characterize a 90nm CMOS technology and to understand effects of technology scaling. Use the model files available on the assignment web-page.

## 1 Problem 1

1. Determine the threshold voltage for the NMOS and the PMOS devices by extrapolating the zero-crossing of their  $I_d - V_{gs}$  characteristic, measured for low value of  $V_{ds}$ . Compare the extrapolated value with the value obtained in HSPICE by performing a .DCOP analysis.
2. Analyze the effect of substrate bias on the threshold voltage. Plot the extrapolated value of threshold voltage for negative and positive body bias in an appropriate range. Extract the body effect coefficient and  $\frac{V_{th}}{V_{sb}}$
3. Analyze the effect of channel length on threshold voltage. Simulate devices with  $W/L=10$  and channel length ranging from  $.1\mu$  to  $2\mu$ . Discuss the obtained results. <sup>1</sup>
4. Draw drain current and threshold voltage as a function of drain bias for an NMOS and a PMOS device. What is the measured DIBL factor ?

## 2 Problem 2 :Speed

1. Measure the delay of a Fan-Out-Of-4 inverter  $T_{FO4}$  as shown in class. Device sizes are NMOS  $.51\mu/.1\mu$ , PMOS  $.88\mu/.1\mu$  for  $V_{dd} = 1V$ . Assuming the maximum logic depth in the circuit is 10(including Flip-Flop Clock-to-Q and setup time) and the average delay through the logic is  $T_{FO4}$ , what is the maximum operating frequency achievable using static CMOS in this process?(As a side note, notice that delay predictions with this model are fairly pessimistic compared to a real 90nm process)
2. Repeat the measurement for  $V_{dd} = [.5 : .05 : 1]$ (MATLAB notation). Using MATLAB, fit the simulated result using the built-in function `lsqcurvefit` and the template `AlphaPowerLaw.m` provided on the website.Repeat for  $V_{dd} = [.1 : .05 : 1]$ . Discuss the obtained results. Under the conditions expressed in the previous point, what is the minimum value of  $V_{dd}$  allowing operation at 64MHz? Please submit parameter value for the Alpha-Power Law delay model as well as plots showing simulated delay and delay predicted by the model.

## 3 Problem 3:Scaling

For this problem, assume that logic gates are ported across different technologies while keeping the  $W/L$  ratio constant. That is if a 90nm inverter is sized  $W_n/L_n = .51\mu/.09\mu, W_p/L_p = .88\mu/.1\mu$  a 65nm inverter will have device sizes  $W_n/L_n = 65/90 \cdot .51\mu/.09\mu, W_p/L_p = 65/90 \cdot .88\mu/.1\mu$ . You will need data from the low-power technology roadmap, which can be found at <http://public.itrs.net>.Download the Process and Device roadmap, edition 2005.

1. Simulate power dissipation of a static CMOS inverter built in 180nm CMOS technology, when the input is a 100MHz square wave with 30ps rise and fall time. Using scaling theory and data from ITRS, predict power dissipation at the 90nm,65nm and 45nm nodes.

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<sup>1</sup> The book *Operation and modeling the MOS transistor* by Y.P.Tsividis is a good reference for this.

2. Using the models posted on the website, simulate at the 90nm,65nm and 45nm nodes. Comment on the results.

#### **4 Problem 4:New Structures**

Read the paper *The end of CMOS Scaling* by T.Skonitki et al.

1. What is the motivation for exploring non-classical transistor structures ?
2. For each of the proposed structures, summarize in a few sentences strong and weak points