EE241 S06 Homework #1Solution

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1 Problem 1

1. *Determine the threshold voltage for the NMOS and the PMOS devices by extrapolating the zero-crossing of their $I_d - V_{gs}$ characteristic, measured for low value of V_{ds}. Compare the extrapolated value with the value obtained in HSPICE by performing a .DCOP analysis.*
   The plot is shown in figure 1. The extracted values of Vt for the NMOS and the PMOS devices are respectively 340mV and 300mV. The vaues obtained from .DC analysis are respectively 275mV for NMOS and 280mV for PMOS.

2. *Analyze the effect of substrate bias on the threshold voltage. Plot the extrapolated value of threshold voltage for negative and positive body bias in an appropriate range. Extract the body effect coefficient and $\frac{\partial V_{th}}{\partial V_{sb}}$*
   A graph of Threhold Voltage versus substrate bias is reported in figure 2. Please notice the limited effect of substrate bias on the threshold voltage(1 V forward bias only gives about 120mV decrease in the threshold. To determine the parameters of the equation $V_{th} = V_{T0} + \gamma(\sqrt{\Phi + V_{sb}} - \sqrt{\Phi})$, I fitted the expression using MATLAB lsqcurvefit function for positive values of substrate bias only. The results are 1.

Device	γ	Φ	V_{T0}
NMOS	.3342	.4547	.2688
PMOS	.3842	1.15	.2833

   Tab. 1: Fitted parameters of threshold voltage model

   The slope of the curve $\frac{\partial V_{th}}{\partial V_{sb}}$ is in figure 3.

3. *Analyze the effect of channel length on threshold voltage. Simulate devices with W/L=10 and channel length ranging from $.1\mu$ to 2μ. Discuss the obtained results.* [1]
   See figure 4 Notice that the devices exhibit both short channel and reverse short channel effect. This is characteristic of transistors built pushing the limits of the process. If you had to extract the same plot for a commercial 90nm process, you would only find reverse short channel effect.

4. *Draw drain current and threshold voltage as a function of drain bias for an NMOS and a PMOS device. What is the measured DIBL factor ?*
   Figure 5 reports the behavior of drain current versus drain bias for an NMOS device biased at $V_{gs} = 0$.

   DIBL changes threshold voltage by means of the interaction between drain and channel potential . The resuling shift in the potential barrier for electrons increases subthrehold current [1].This effect can be modeled as

   $$I_d \mid_{V_{gs}=0} = I_0 \exp \frac{-V_{TH} + \sigma V_{ds}}{n(KT/q)} \quad (1)$$

   Where K is Boltzmann's constant, T is the absolute temperature and q is the electron charge, while I_0 is a technological paramater. In equation 1, it is assumed $V_{ds} > 125mV$, so that the device does

[1] The book *Operation and modeling the MOS transistor* by Y.P.Tsividis is a good reference for this.

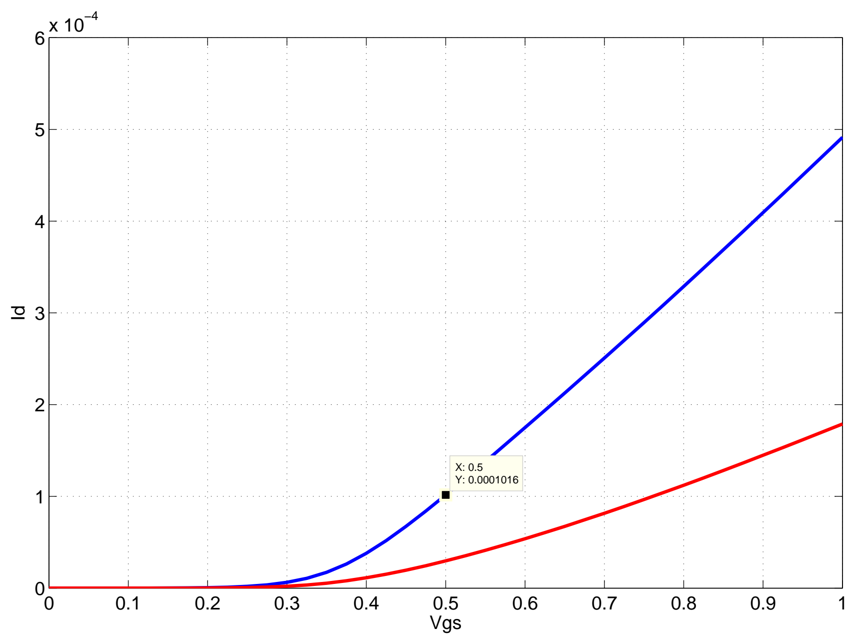

Fig. 1: I-V characthrestics of NMOS and PMOS devices

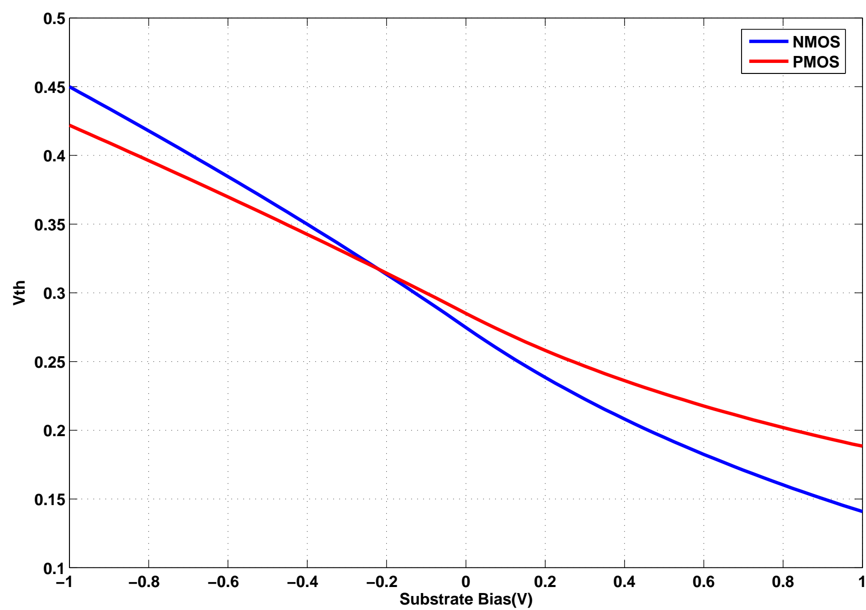

Fig. 2: Simualted threshold voltge versus substrate bias

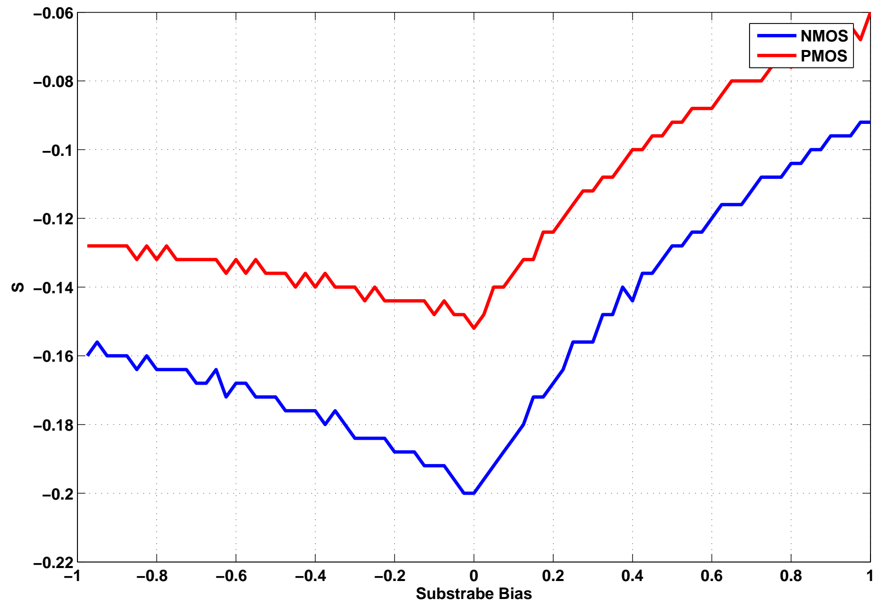

Fig. 3: $\frac{\partial V_{th}}{\partial V_{sb}}$ extracted from simulation

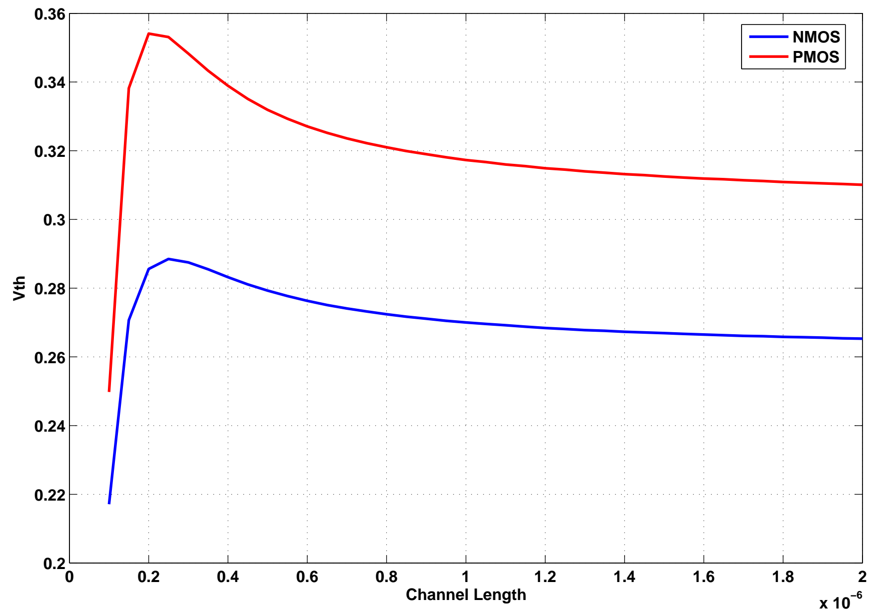

Fig. 4: Threshold voltage dependence on channel length

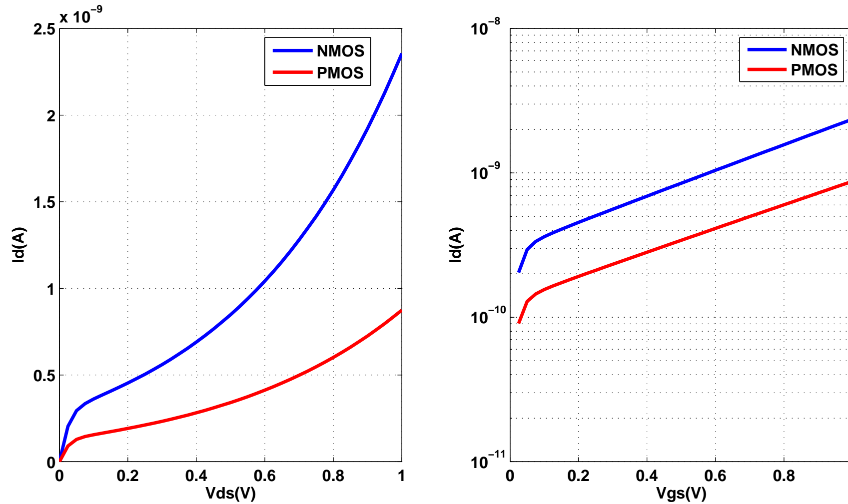

Fig. 5: $I_d - V_{ds}$ curves for the 90nm CMOS models

not operate in the triode region. To extract the coefficient σ, an intuitive method is used. Taking the logarithm of the left and the rigth side of equation 1,

$$\log I_d = \log I_0 - \frac{-V_{TH} + \sigma V_{ds}}{n(KT/q)}$$

is obtained. Therefore, $\frac{\partial \log I_d}{\partial V_{ds}} \cdot \frac{nKT}{q} = \sigma$. The results are in table 2

Device	σ
NMOS	.08
PMOS	.076

Tab. 2: Fitted parameters of drain induced barrier model

2 Problem 2 :Speed

1. *Measure the delay of a Fan-Out-Of-4 inverter T_{FO4} as shown in class. Device sizes are NMOS $.51\mu/.1\mu$, PMOS $.88\mu/.1\mu$ for $V_{dd} = 1V$. Assuming the maximum logic depth in the circuit is 10(including Flip-Flop Clock-to-Q and setup time) and the average delay through the logic is T_{FO4}, what is the maximum operating frequency achievable using static CMOS in this process?(As a side note, notice that delay predictions with this model are fairly pessimistic compared to a real 90nm process)*
Using the schematic seen in class, I extracted a $T_{FO4} = 54pS$. This results in $F_{Max} = \frac{1}{10 \cdot T_{FO4}} = 1.85GHz$.

2. *Repeat the measurement for $V_{dd} = [.5 : .05 : 1]$(MATLAB notation). Using MATLAB, fit the simulated result using the built-in function lsqcurvefit and the template AlphaPowerLaw.m provided on the website.Repeat for $V_{dd} = [.1 : .05 : 1]$. Discuss the obrained results. Under the conditions expressed in the previous point, what is the minimum value of V_{dd} allowing operation at 64MHz? Please submit parameter value for the Alpha-Power Law delay model as well as plots showing simulated delay and delay predicted by the model.* Figure 6 contains the measured delay against $V_{dd} = [.1 : .05 : 1]$. By fitting ony the portion for $V_{dd} = [.5 : .05 : 1]$ using the α-Power Law model, I found the values reported in table 3,line 1. Repeating for the data for $V_{dd} = [.1 : .05 : 1]$ results in the parameters in line 2 of the same table. Convergence issues result complex, physically meaningless values. This is due to the exponential dependence of delay on V_{dd} for low supply. Extracting(from the measured delay), the point corresponding to $F_{clk} = 64MHz$, $V_{dd} =$ is obtained.

Range	V_{TH}	α	K
[.5 : .05 : 1]	.3894	1.24	.5872
[.1 : .05 : 1]	.38-1e-3i	1.2362-.0112i	.5114 -.037i

Tab. 3: Fitted parameters of α-power law delay model

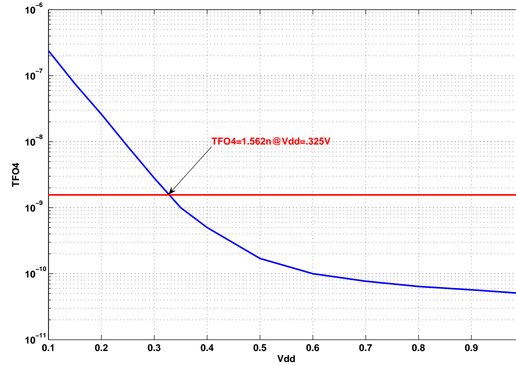

Fig. 6: FO4 Inverter delay as a function of supply voltage

3 Problem 3:Scaling

For this problem, assume that logic gates are ported across different technologies while keeping the W/L ratio constant. That is if a 90nm inverter is sized $W_n/L_n = .51\mu/.09\mu$,$W_p/L_p = .88\mu/.1\mu$ a 65nm inverter will have device sizes $W_n/L_n = 65/90 \cdot .51\mu/.09\mu$, $W_p/L_p = 65/90 \cdot .88\mu/.1\mu$. You will need data from the low-power technology roadmap, which can be found at http://public.itrs.net.Download the Process and Device roadmap, edition 2005.

1. *Simulate power dissipation of a static CMOS inverter built in 180nm CMOS technology, when the input is a 100MHz square wave with 30ps rise and fall time. Using scaling theory and data from ITRS, predict power dissipation at the 90nm,65nm and 45nm nodes.*
   I simulated a chain of 3 identical inverters,with $W_n/L_n = 1\mu/.18\mu; W_p/L_p = 1.76\mu/.18\mu$ and tied the supply of the first inverter to a different voltage source than the supply of the second and the third. The measured average(over 5 μS) current through the supply of the first inverter was $1.88\mu A$, corresponding to $P_d = 3.4\mu W$. Scaling from 180nm to 90nm is constant field, while scaling beyond 90n requires generalized scaling theory. Parameters used are taken from the ITRS roadmap and reported in table 4

Technology Node	V_{dd}	$t_{ox}(nm)$	$\hat{P}_d = \frac{\epsilon_0\epsilon_{ox}}{t_{ox}} V_{dd}^2(W_nL_n + W_pL_p)$	$P_d = V_{dd} \cdot I_{avg}$	P_{leak}
180nm	1.8	3.7	$3.4\mu W$	$3.4\mu W$	1.8nW
90nm	1	1.8	$.53\mu W$	$.36\mu W$	2.5nW
65nm	.8	1.2	$.28\mu W$	$.27\mu W$	20nW
45nm	.7	1	$.12\mu W$	$.56\mu W$	48nW

Tab. 4: Predicted and simulated power dissipation at the different technological nodes

2. *Using the models posted on the website, simulate at the 90nm,65nm and 45nm nodes. Comment on the results.* Inaccuracies derive from 2 major sources:possible discrepancy between the process parameters in a areal process and ITRS predictions.Secondly,a number of parameteres is not included in the scaling law used: in particular Drain/Source capacitance scales linearly or sub-linearly with channel length and may dominate over gate capacitance at extremely small lengths. Notice that leakage is also not included in the scaling law, but due to relaitvely fast operation its contribution is only relevant in the 45nm node

4 Problem 4:New Structures

Read the paper *The end of CMOS Scaling* by T.Skonitki et al.

1. What is the motivation for exploring non-classical transistor structures ?
2. For each of the proposed structures, summarize in a few sentences strong and weak points

References

[1] Liu, Z.-H.; Hu, C.; Huang, J.-H.; Chan, T.-Y.; Jeng, M.-C.; Ko, P.K.; Cheng, Y.C. *Threshold voltage model for deep-submicrometer MOSFETs* Electron Devices, IEEE Transactions on Volume 40, Issue 1, Jan. 1993 Page(s):86 - 95