

EE241 Homework #2

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The goal of this assignment is to compare different logic styles in 90nm CMOS.

1 Problem 1

The AOI4 gate is a complex gate that finds wide use in today's standard cell library. Its functionality is defined by $Z = \overline{AB + CD}$.

1. Design such a gate in static CMOS. Device sizes will be $W_n/L_n = .22\mu/.09\mu$, $W_p/L_p = .51\mu/.09\mu$. Measure energy, delay and energy-delay product. The cell inputs should be driven by unit inverters, the cell output should be loaded with 4 unit inverters to suppress overshoot.
2. Redesign the same gate using DCVSL. Use the karnaugh map technique to synthesize the complementary pull down networks, for which you will use NMOS devices sized as $W_n/L_n = .22\mu/.09\mu$. Sweep the width of the PMOS cross-coupled load and plot delay, energy and energy-delay. What is the optimal width value from an energy perspective? What about energy-delay?
3. Repeat the previous point, but instead of using a cross-coupled load, put an inverter at the end of each chain, followed by a keeper with the gate tied to the inverter output.

2 Problem 2:PS-CMOS

1. Design a three-inputs XOR gate using the PS-CMOS logic style
2. Size the gate for optimum performance using logical effort analysis. Assume that each device within a NAND or NOR gate has the same size.

3 Problem 3:Timing in Pass-Transistor logic

Consider the circuit shown in figure 1. Assume $V_{Tn} = |V_{Tp}| = 300mV$.

1. Derive the minimum supply such that the circuit is still operational
2. Determine the critical path, and give an expression for its delay (Hint: you RC modeling and Elmore Delay Model)
3. Discuss power dissipation of this circuit. Is there a problem?
4. Discuss available strategies to overcome the limitations highlighted in the previous point and their impact on power dissipation and delay

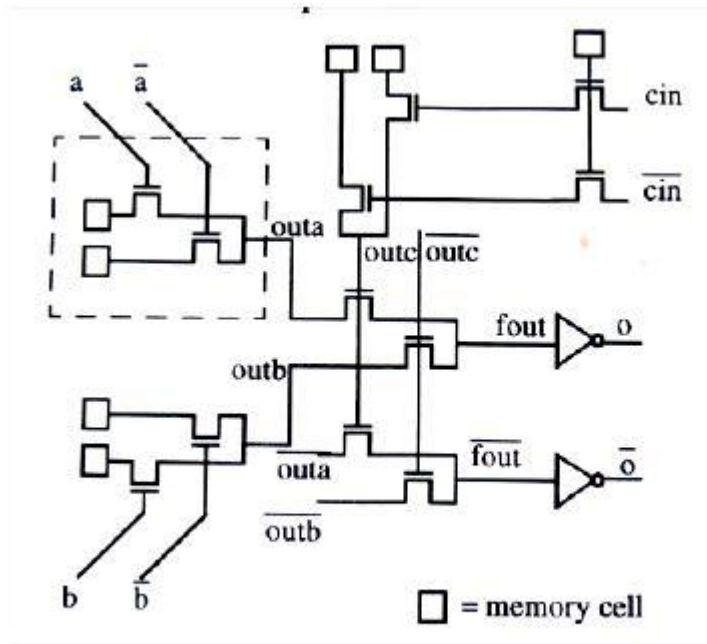


Fig. 1: Circuit schematic for problem 3