

EE241 Homework #3

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In this assignment we'll discuss dynamic logic design and power aware design

1 Problem 1

Design a domino gate to implement the logic function $NOT(NOT(A + B)NOT(CNOT(D) + CD))$.

2 Problem 2: Voltage Scaling

In this problem, we'll compare different technologies from an energy-per operation point of view.

Assume that you are building an ASIC, and that your critical path is a chain of six(6) NAND2 gates, driving a 20 unit inverter load.

1. Optimize this gate chain using logical effort analysis. Simulate worst case delay and verify that it meets $t_p \ll 5nS$. Annotate leakage power for this circuit with this particular(worst case delay) input vector.
2. Under the assumption that all nodes in the circuit have a switching activity of α_1 , give an expression for the active power dissipation of the circuit. Evaluate this expression for $\alpha_1 = .1, .01, .001$
3. In problem 1, HW1, we found the parameters for α -power law delay model of the 90nm predictive technology model. Using such a model, and assuming that adder delay scales with voltage the same way as inverter delay, derive an approximate value of V_{dd} such that your circuit will meet exactly the $t_p = 5ns$ specification. Using the expression previously derived, estimate the active power consumption at this new voltage level. Using the DIBL coefficient derived in HW1, estimate the new leakage power.
4. You have the opportunity to redesign your ASIC. This time, you can choose to use the bulk 90nm technology, or a process option with .1V thresholds, with 30% lower delay at $V_{dd} = 1V$, but 500 times higher leakage. For this technology, delay is well modeled by alpha-power law with parameters $alpha = 1.24, V_{th} = .1, K = .5872$. (i.e. $t_d(V_{dd}) = t_d(V_{dd} = 1) \frac{.8772}{(V_{dd} - .1)^{1.24}}$, $t_d(V_{dd} = 1) = 38.5pS$). Your delay spec is the same-you only care about power. For each of the previous scenarios (i.e. activity $alpha_1 = .1, .01, .001$), what technology do you choose?

3 Problem 3

Read the paper *Boost Logic: A High Speed Energy Recovery Circuit Family* (<http://ieeexplore.ieee.org/search/wrapper.jsp?arnumber=1430105>), by V.Sathe, M.Papaefthymiou and C.Ziesler, in Proceedings of IEEE Computer Society Annual Symposium on VLSI. The authors propose an implementation of an high speed, energy recovery implementation of the interesting concept of having low-swing logic following by level restoring sense amplifiers.

- Summarize the main strong and weak points of the proposed logic style
- Explain how the circuit performance and power dissipation would change if the boost stage were replaced by a more conventional CMOS sense amplifier with a reset and latch phase controlled by a synchronous clock