

EE241 Homework #4

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In this assignment we'll discuss timing concepts and SRAM design. There are a few SRAM papers posted on the website, you might want to check them out.

1 Problem 1

Consider a simplified model of a memory element as shown in 1:

I1 and I2 have the same sizes and they are designed in our 90nm predictive model. Specifically, PMOS size is $.2\mu/.1\mu$, while NMOS are sized to be $.12\mu/.09\mu$.

1. Assume that A=1 is stored in the memory when V_{dd} . Plot the voltage at nodes A and B for V_{dd} decreasing from 1V down to 0. The value at which the cell loses its state is called Data Retention Voltage(DRV). What is the DRV for this cell ?
2. Now, analyze the effect of process variations. The process exhibits $\pm 6\text{nm}$ variations in channel length. Analyze what is the worst case variation (the one that gives highest DRV). Simulate to verify your hypothesis.
3. It is known that variations can be counteracted by increasing transistor size or employing Adaptive body biasing. You can therefore: a) increase the length/width of the NMOS devices b) increase the length/width of the PMOS devices c) Control NMOS body bias voltage d) control PMOS body bias voltage. Discuss pros/cons each of these techniques. The main metrics of interest are cell area, leakage power and eventual overhead.

2 Problem 1: Ling Adder

Read the paper *A subnanosecond .5 μ Adder Design* by S.Naffziger, ISSCC 1996(posted). Reconstruct the key Ling adder logic equations(the equations that relate the inputs to the outputs of the adder). Draw the parallel-prefix tree implemented in this adder.

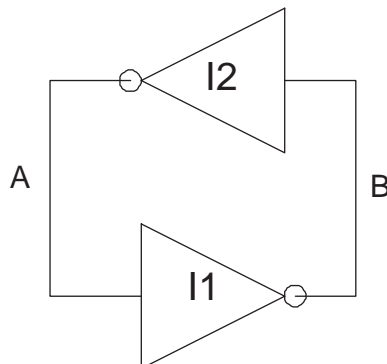


Fig. 1: Simplified SRAM cell

3 Problem 3

A synchronous mixed signal chip uses the same clock-rate of 1GHz in both the analog and the digital sections, but different clock trees. Insertion delay of the analog clock tree is $1.2ns \pm .1ns$, while insertion delay of the digital adder is $1.5ns \pm .1ns$. Label Φ_1 the analog clock and Φ_2 the digital clock. The ADC output is sampled by a register bank clocked by Φ_1 , fed into a combinational logic stage, and sampled by a register bank clocked by Φ_2 . Φ_1 and Φ_2 have $\pm 50pS$ of relative skew. The Flip-Flops have $T_{su} = 50pS, T_h = 75pS, T_{CQ} = 120pS$. Calculate the maximum and minimum delay of the combinational block that guarantee correct system operation.