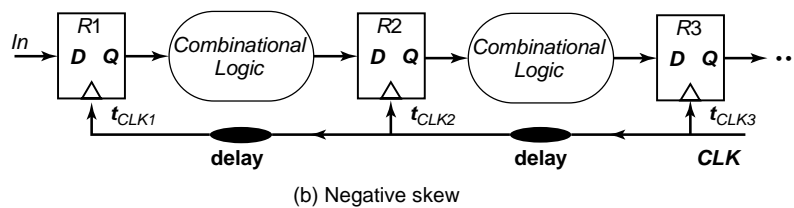
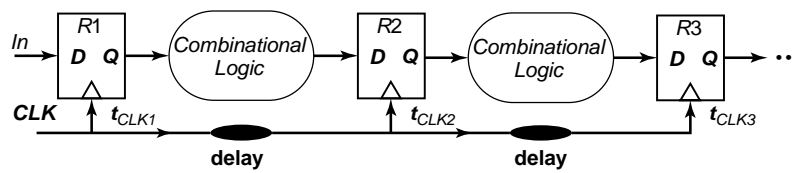


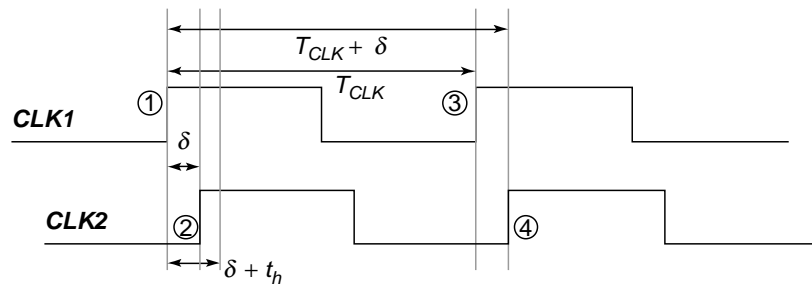
# EE241 - Spring 2006 Advanced Digital Integrated Circuits

## Lecture 19: Timing + Asynchronous

### Positive and Negative Skew



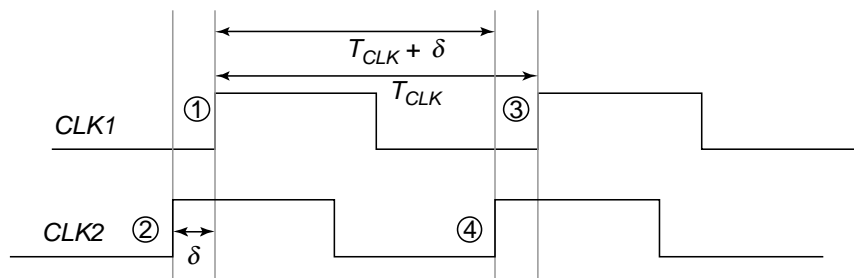
## Positive Skew



*Launching edge arrives before the receiving edge*

3

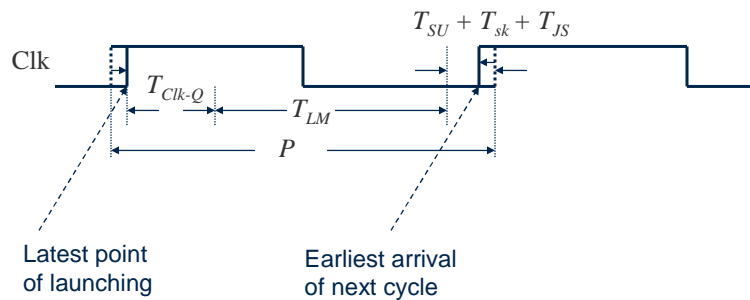
## Negative Skew



*Receiving edge arrives before the launching edge*

4

## Longest Logic Path in Edge-Triggered Systems



Unger and Tan  
Trans. on Comp.  
10/86

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## Clock Constraints in Edge-Triggered Systems

If launching edge is late and receiving edge is early, the data will not be too late if:

$$P - T_{sk} + T_{JS} - T_{SU} \geq T_{clk-QM} + T_{LM}$$

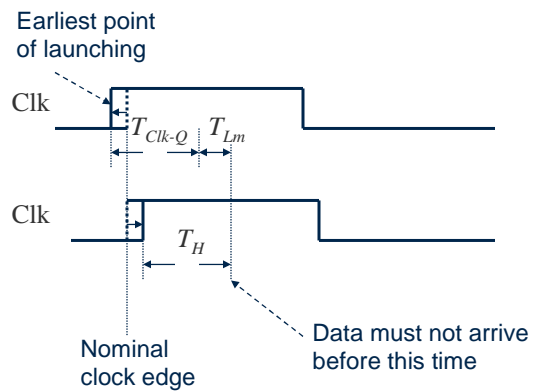
Minimum cycle time is determined by the maximum delays through the logic

$$P \geq T_{clk-QM} + T_{LM} + T_{SU} + T_{sk} + T_{JS}$$

'Double-sided' definitions of setup and jitter

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## Shortest Path



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## Clock Constraints in Edge-Triggered Systems

If launching edge is early and receiving edge is late:

$$T_{clk-Qm} + T_{Lm} \geq T_{sk} + T_H$$

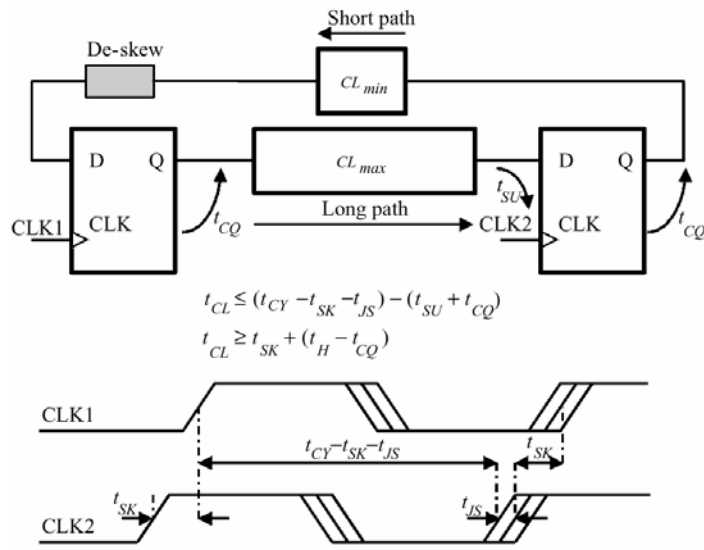
Minimum logic delay

$$T_{Lm} \geq T_{sk} + T_H - T_{clk-Qm}$$

Jitter does not really play as this concerns the same clock edge

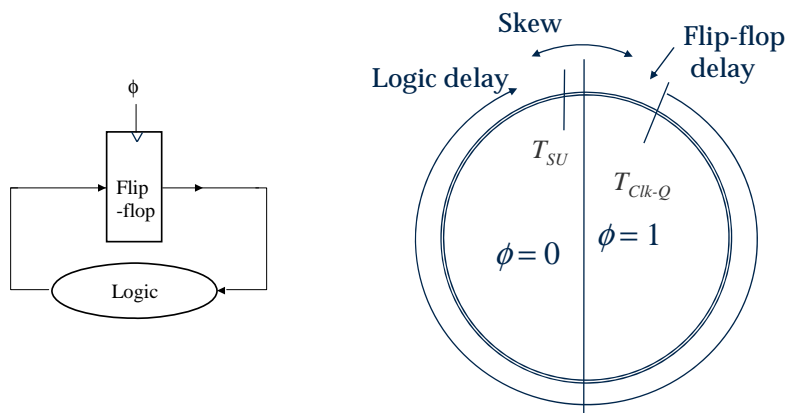
8

## Clock Constraints in Edge-Triggered Systems



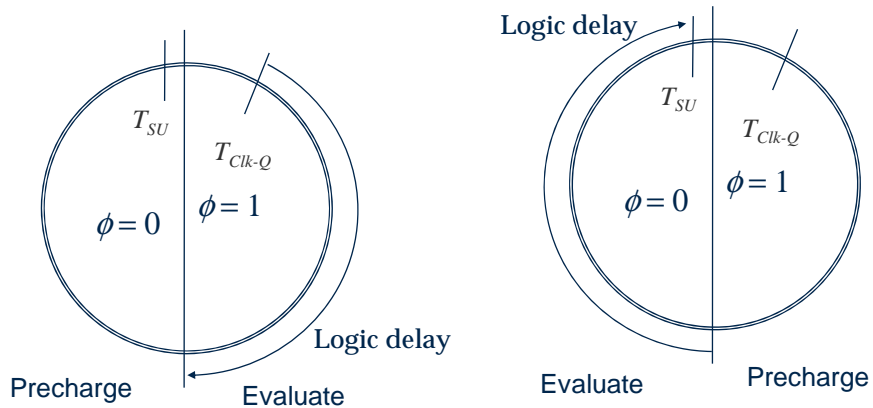
Courtesy of IEEE Press, New York. © 2000

## Flip-Flop – Based Timing



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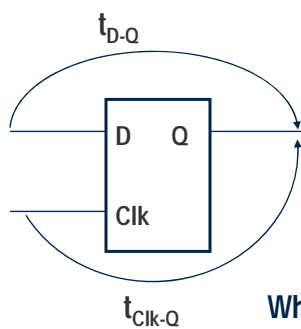
## Flip-Flops and Dynamic Logic



Flip-flops are used only with static logic  
No way to hide the precharge overhead

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## Latch timing



When data arrives  
to transparent latch

Latch is a 'soft' barrier

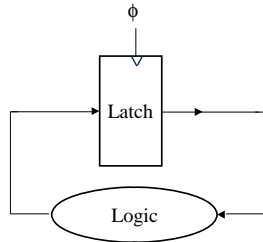
When data arrives  
to closed latch

Data has to be 're-launched'

Latch insensitive to skew/jitter in transparent zone

12

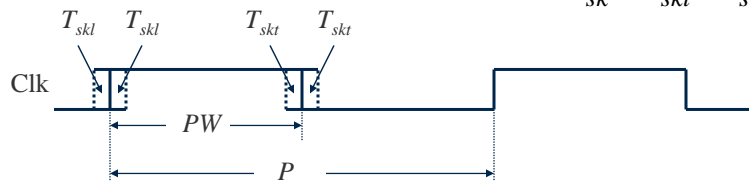
# Single-Phase Clock with Latches



Unger and Tan  
Trans. on Comp.  
10/86

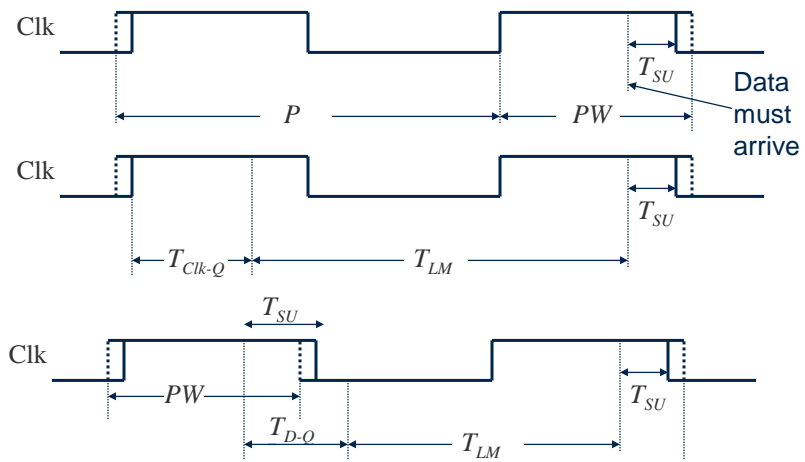
In Chapter 11:

$$T_{sk} = T_{skl} + T_{skt}$$



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# Preventing Late Arrivals



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## Preventing Late Arrivals

$$P \geq \max \left\{ \begin{array}{l} T_{skl} + T_{skt} + T_{SU} + T_{clk-QM} - PW, \\ T_{D-QM} \end{array} \right\} + T_{LM}$$

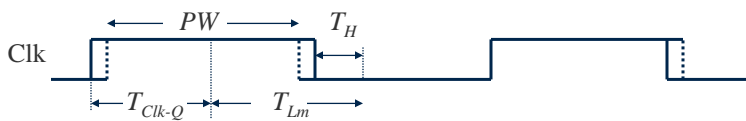
Or:

$$P \geq T_{clk-QM} + T_{LM} + T_{SU} + T_{skl} + T_{skt} - PW$$

$$P \geq T_{D-QM} + T_{LM}$$

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## Preventing Premature Arrivals



Two cases, reduce to one:

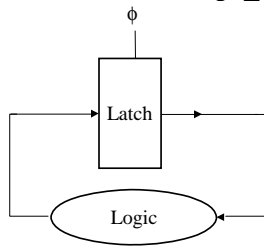
$$T_{Lm} \geq T_{skl} + T_{skt} + T_H + PW - T_{Clk-Qm}$$

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## Single-Latch Timing

Bounds on logic delay:

$$P \geq \max \left\{ T_{skl} + T_{skt} + T_{SU} + T_{clk-QM} - PW, T_{D-QM} \right\} + T_{LM}$$



$$T_{Lm} \geq T_{skl} + T_{skt} + T_H + PW - T_{Clk-Qm}$$

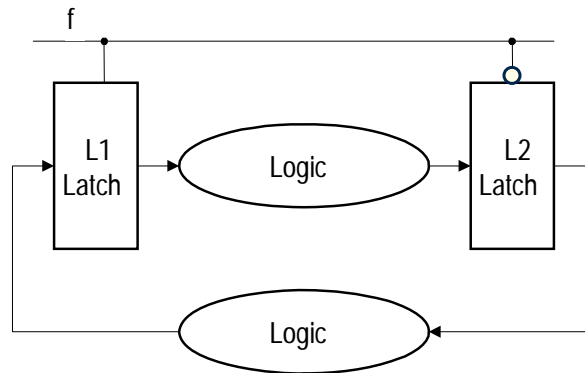
Either balance logic delays  
or make PW short

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## Latch-Based Design

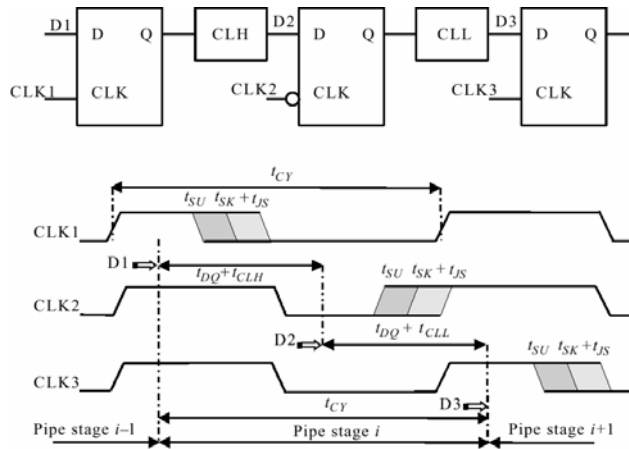
L1 latch is transparent  
when  $f = 1$

L2 latch is transparent  
when  $f = 0$



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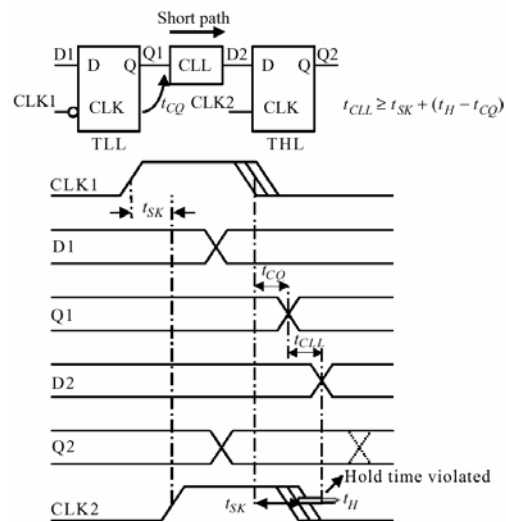
## Latch-Based Timing



As long as transitions are within the assertion period of the latch, no impact of position of clock edges

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## Latch Design and Hold Times



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## Latch-Based Timing

➤ Longest path

$$P \geq 2T_{D-QM} + T_{LHM} + T_{LLM}$$

*Independent of skew*

● Short paths

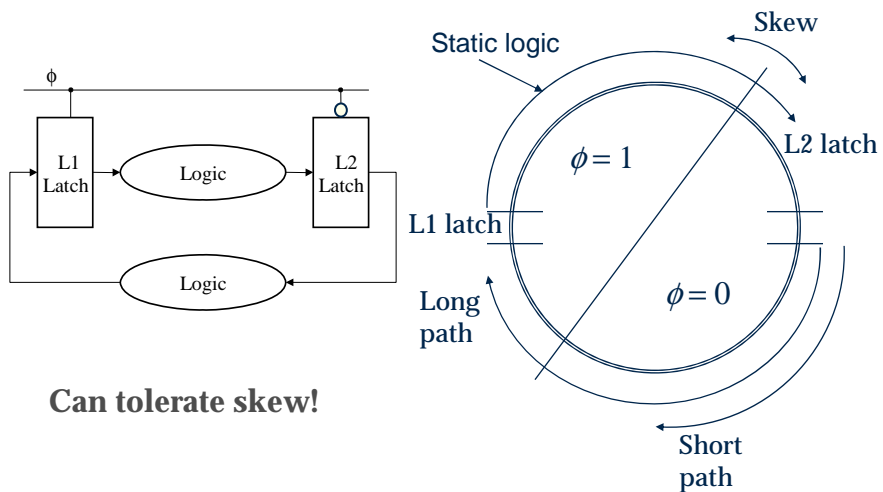
$$T_{CLLm} \geq T_{SK} + T_H - T_{Clk-Qm}$$

$$T_{CLHm} \geq T_{SK} + T_H - T_{Clk-Qm}$$

*Same as register-based design but holds for both clock edges*

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## Latch-Based Timing



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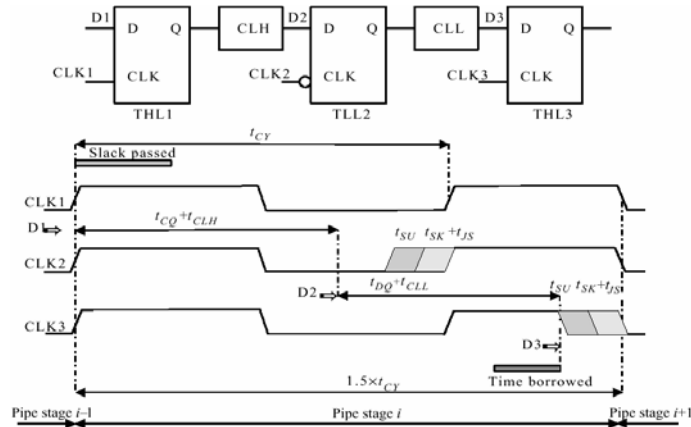
## Soft-Edge Properties of Latches

- **Slack passing** – logical partition uses left over time (slack) from the *previous* partition
- **Time borrowing** – logical partition utilizes a portion of time allotted to the *next* partition
- Makes most impact in unbalanced pipelines

Bernstein et al, Chapter 8, Partovi, Chap 11

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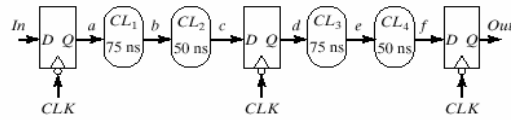
## Slack-Passing and Cycle Borrowing



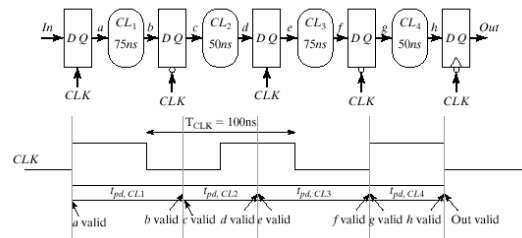
For  $N$  stage pipeline, overall logic delay should be  $< N T_{cl}$

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# Slack Passing Example

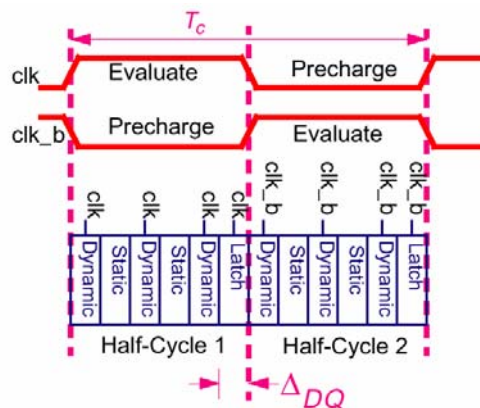


Edge Triggered:  
T = 125 nsec



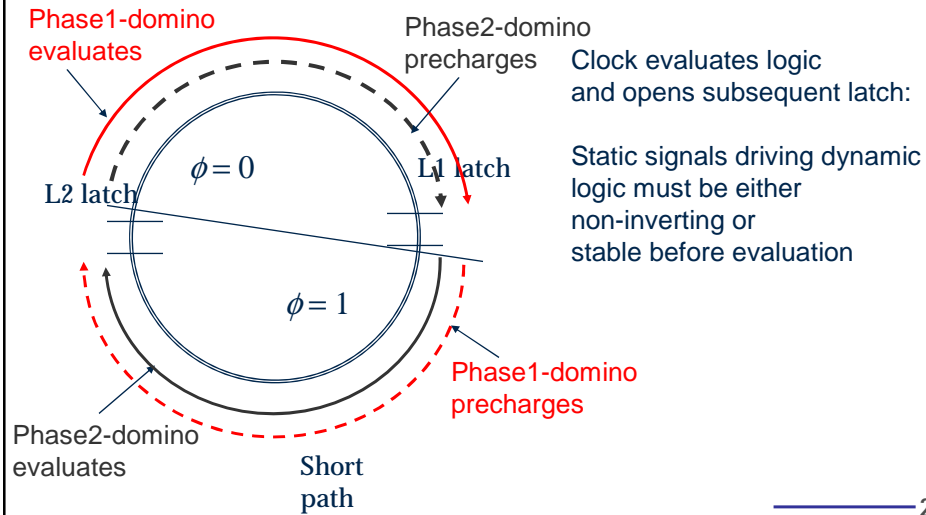
Latch-based:  
T = 100 nsec

# Domino Logic with Latches

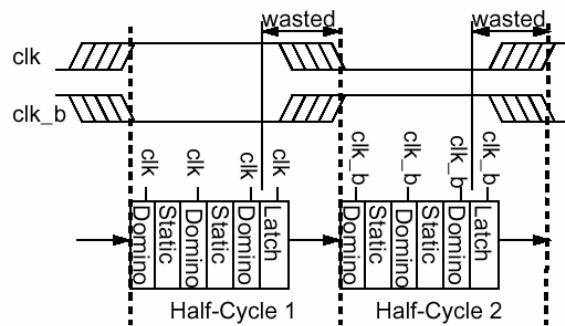


Time available to logic is  $P - 2T_{D-Q}$

## Latches with Dynamic Logic



## Clock Skew in Dynamic

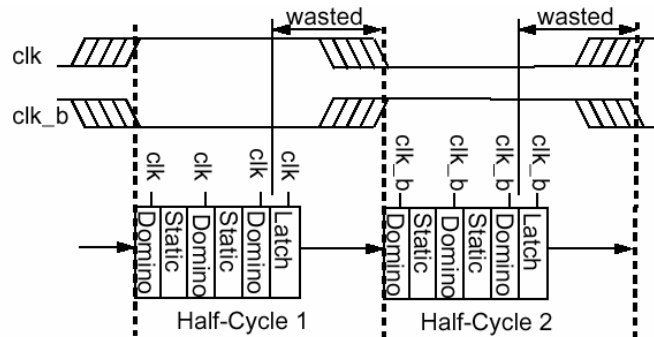


- Evaluation begins at latest rising edge
- Latch input setup before earliest falling edge
- Clock skew twice each cycle

Time penalty:  $T_L = P - (2T_{D-Q} + 2T_{sk})$

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## Non-Balanced Phase Delays



Logic may not exactly fit half-cycle

- No flexibility to borrow time

$$\text{Time penalty: } T_L = P - (2T_{D-Q} + 2T_{sk}) - T_{imbal}$$

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## Skew-Tolerant Domino

### ➤ General Reference:

Harris, Horowitz, "Skew-tolerant domino circuits"  
ISSCC'97, JSSC 11/97

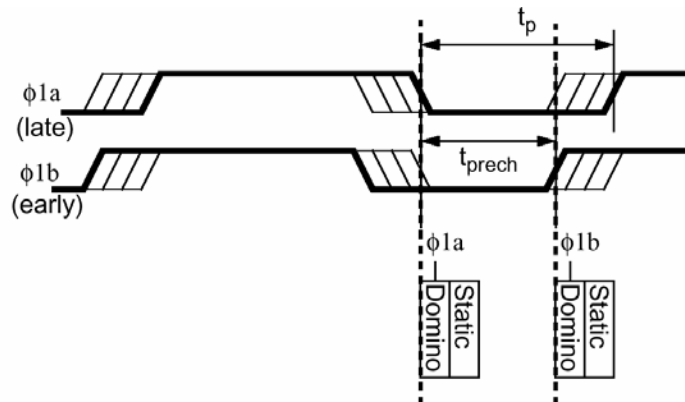
Also slides from D. Harris's Web site:

<http://www3.hmc.edu/~harris/index.html>

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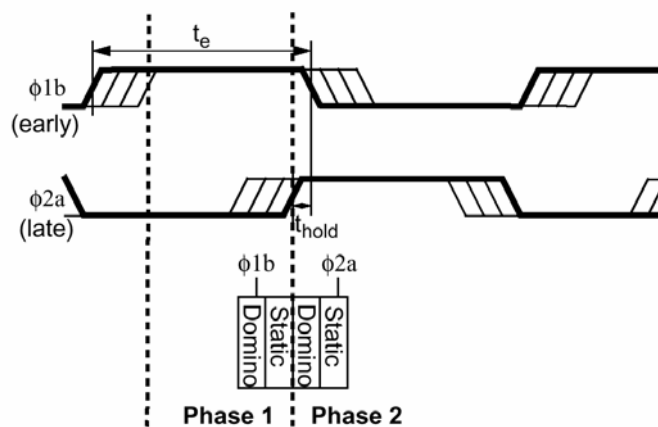
## Precharge Phase



Precharge:  $t_p = t_{prech} + t_{skew}$

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## Evaluation Phase



Overlap:  $t_e = T/N + t_{skew} + t_{hold}$

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## Skew Tolerance

We've found the optimal duty cycle

- Precharge:  $t_p = t_{prech} + t_{skew}$
- Overlap:  $t_e = T/N + t_{skew} + t_{hold}$

Solve for the maximum tolerable skew

$$\bullet t_{skew-max} = \frac{N-1}{N} T - t_{prech} - t_{hold}$$

- Skew tolerance increases with N

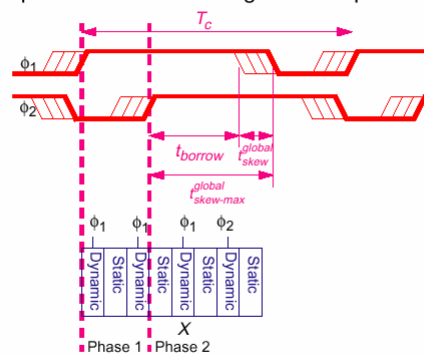
From [Harris]

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## Time Borrowing

Time borrowing

- Excess overlap allows time borrowing into next phase (e.g. gate X)



$$\bullet t_{borrow} = t_{skew-max}^{global} - t_{skew}^{global} = \frac{N-1}{N} T_c - t_{prech} - t_{hold} - t_{skew}^{local} - t_{skew}^{global}$$

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## Self-timed Design

### Reading

- Chapter 9, Self-Timed Pipelines, by T. Williams
- Chapter 10 in Rabaey et al

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## Self-timed and Asynchronous Design

### Functions of clock in synchronous design

- 1) Acts as completion signal
- 2) Ensures the correct ordering of events

### Truly asynchronous design

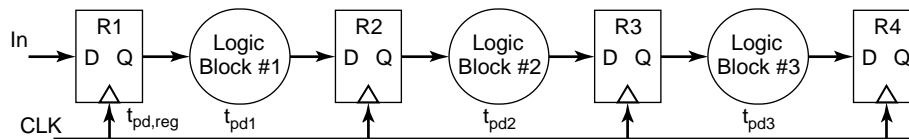
- 1) Completion is ensured by careful timing analysis
- 2) Ordering of events is implicit in logic

### Self-timed design

- 1) Completion ensured by completion signal
- 2) Ordering imposed by handshaking protocol

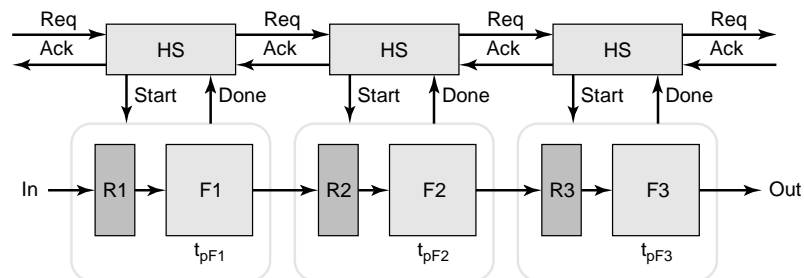
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## Synchronous Datapath



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## Self-Timed Pipelined Datapath



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