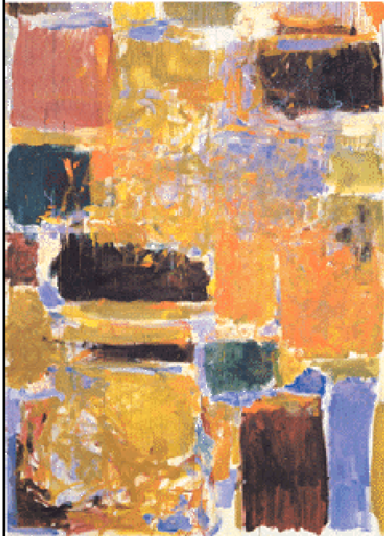
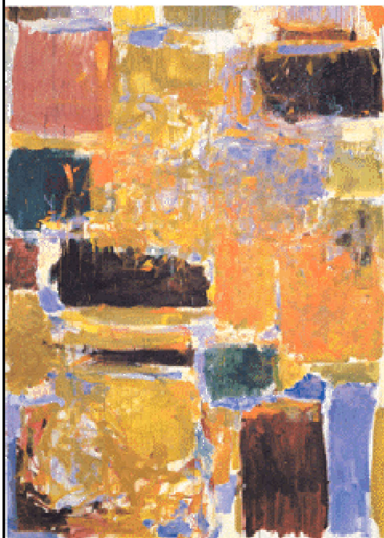


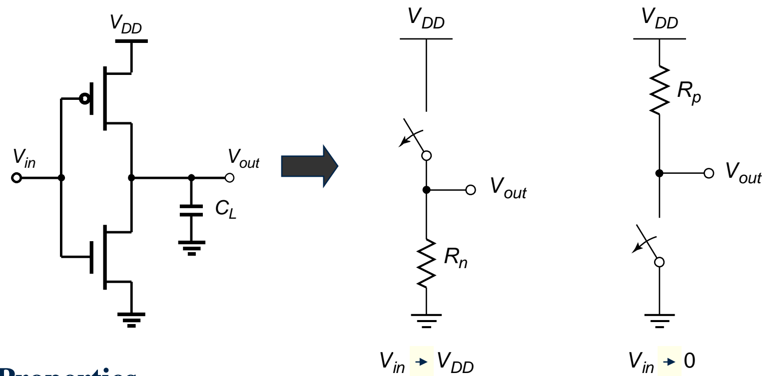
EE241 - Spring 2006
Advanced Digital Integrated Circuits

Lecture 2:
Scaling and Modeling



Device Models

Basic CMOS Gate



Properties

- **Output levels determined by supply**
- **Large noise margins**
- **Performance loss at low voltages (overdrives)**

3

Digital Gate

Basic Properties

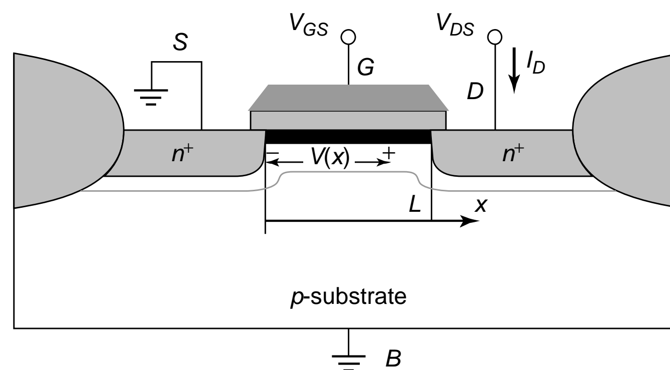
- **Functionality**
- **Area (Cost)**
  - **Density**
- **Robustness**
  - **Δ Swing, Noise margins, Noise sensitivity**
- **Delay**
  - t_{PLH}, t_{PHL}
- **Power, energy consumption**

4

Transistor Models

- In this class we will use a variety of transistor models
- Always use the simplest one needed to analyze a particular effect

The MOS Transistor



MOS transistor with biasing

Transistor Modeling

- Different levels:
  - Hand analysis
  - Computer-aided analysis (e.g. Matlab)
  - Switch-level simulation (e.g. TimeMill)
  - Circuit simulation (Hspice)
- These levels have different requirements in complexity, accuracy and speed of computation
- We are primarily interested in delay and energy modeling, rather than current modeling
- But we have to start from the currents

7

MOS Current

- Vertical field set by V_{GS} induces channel charge
- Gradual charge in the channel is assumed
- Fixed charge in the channel is completely cancelled at $V_{GS} = V_{Th}$
- Charge in the channel is

  $$Q_n = C_{ox}(V_{GS} - V_{Th} - V_C(x))$$
- By Ohm's law,

  $$I_{DS} = WQ_n(x)v = WC_{ox}(V_{GS} - V_{Th} - V_C(x))\,\mu E$$
- Also $E = dV_C(x)/dx$
- Key assumption is that $v = \mu E$, and mobility (μ) is constant

8

MOS Current

$I_{DS} = WC_{ox}(V_{GS} - V_{Th} - V_C(x))\ \mu E$

$I_{DS} = WC_{ox}(V_{GS} - V_{Th} - V_C(x))\ \mu(V_C(x)/dx)$

- When integrated over the channel:

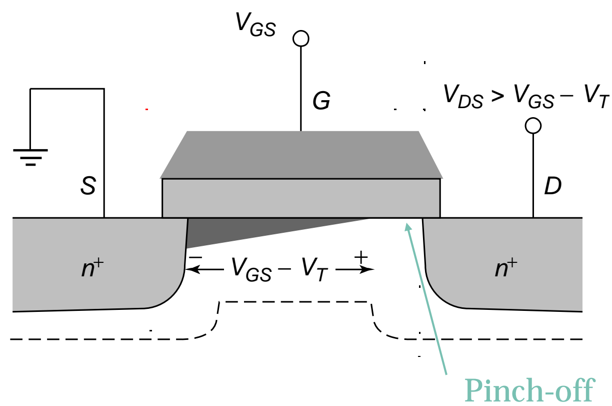
$$I_{DS} = \frac{W}{L}\mu C_{ox}\left(V_{GS} - V_{Th} - \frac{V_{DS}}{2}\right)V_{DS}$$

- Transistor saturates when $V_{GD} = V_{Th}$, - the channel pinches off at drain's side.

$$I_{DS} = \frac{W}{2L}\mu C_{ox}(V_{GS} - V_{Th})^2$$

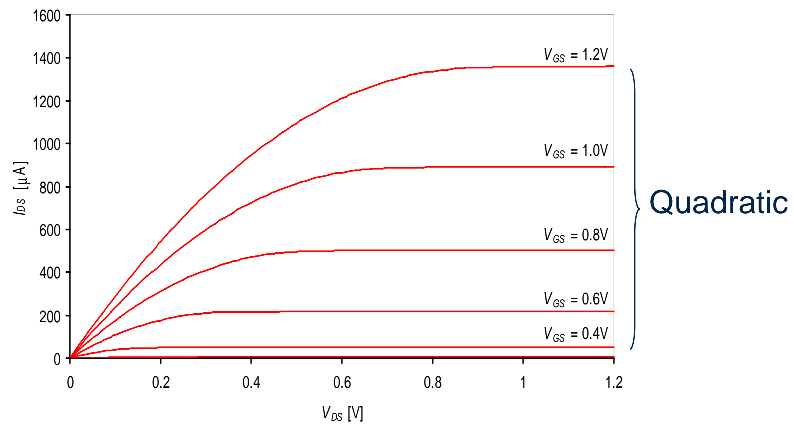
9

MOS Current



10

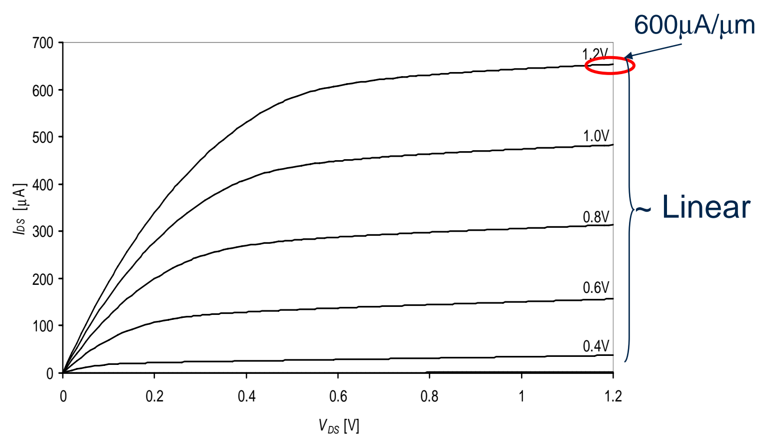
MOS Currents



Currents according to the quadratic model
Correct for long channel devices (L ~ μm)

11

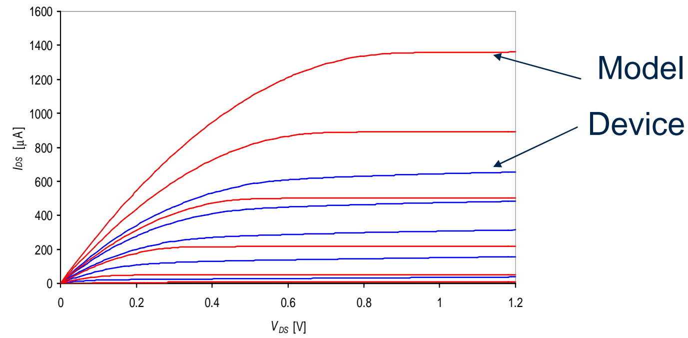
Simulated 0.13μm Transistor



L = 0.13μm

12

Simulation vs. Model

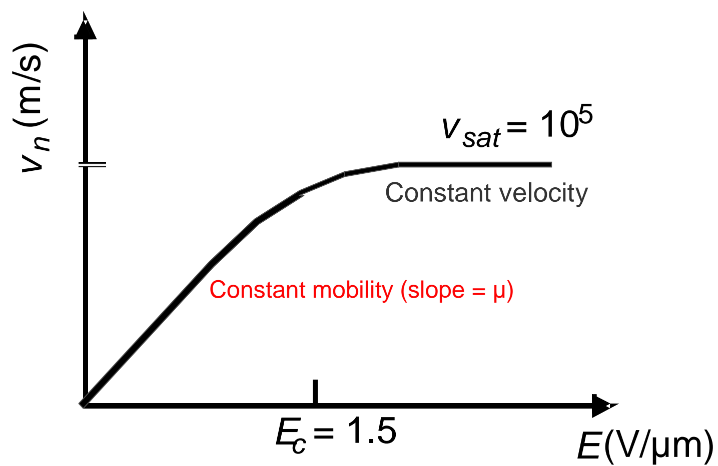


Major discrepancies:

- shape
- saturation points
- output resistances

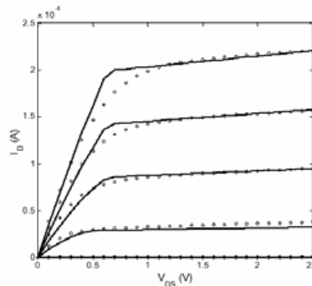
13

Velocity Saturation



14

Unified MOS Equations



From EECS141
Rabaey, 2nd ed.

$$I_D = \begin{cases} 0, & V_{GS} < V_{TH} \\ k'\frac{W}{L}\left((V_{GS}-V_{TH})V_{DS}-\frac{V_{DS}^2}{2}\right), & V_{GS} > V_{TH}, V_{DS} > V_{GS}-V_{TH}, V_{DSAT} > V_{GS}-V_{TH} \\ \frac{k'}{2}\frac{W}{L}(V_{GS}-V_{TH})^2, & V_{GS} > V_{TH}, V_{DS} > V_{GS}-V_{TH}, V_{DSAT} < V_{GS}-V_{TH} \\ k'\frac{W}{L}\left((V_{GS}-V_{TH})V_{DSAT}-\frac{V_{DSAT}^2}{2}\right), & V_{GS} > V_{TH}, V_{DS} > V_{GS}-V_{TH}, V_{DSAT} > V_{GS}-V_{TH} \end{cases}$$

MOS Models

G, S, D, B, I_D

$$I_D = 0 \text{ for } V_{GT} \le 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min}-\frac{V_{min}^2}{2}\right)(1+\lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

$V_{GT} = V_{GS} - V_T$,

and $V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$

γ - body effect parameter

From EECS141
Rabaey, 2nd ed.

Unified MOS Model

- Model presented is compact and suitable for hand analysis.
- Still have to keep in mind the main approximation: that V_{DSat} is constant . When is it going to cause largest errors?
  - When E scales – transistor stacks.
- But the model still works fairly well.

Velocity Saturation

- Velocity is not always proportional to field
- Modeled through variable mobility (mobility degrades at high fields)

$$v = \frac{\mu_{eff} E}{\left(1 + \left(\frac{E}{E_0}\right)^n\right)^{1/n}}$$

$$E_0 = \frac{2 v_{sat}}{\mu_{eff}}$$

NMOS: $n = 2$
PMOS: $n = 1$

- Hard to solve for n =2
- Assume n = 1 (close enough)

[Sodini84]

Velocity Saturation

- When does a transistor enter velocity saturation?

$$V_{DSat} = \frac{(V_{GS} - V_{Th})E_C L}{(V_{GS} - V_{Th}) + E_C L}$$ [Taur, Ning]

- E_C is a function of vertical field, ~linearly proportional to V_{GS}

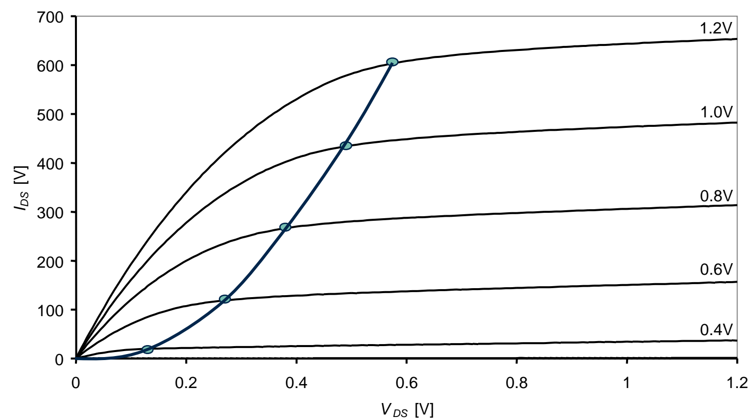
Velocity Saturation

- In 0.13µm technology, $E_C L$ is about $0.5 V_{GS} + 0.7V$
- Can calculate V_{DSat} (V_{Th} ~ 0.25V)

V_{GS} [V]	0.2	0.4	0.6	0.8	1.0	1.2
V_{DSat} [V]	0	0.13	0.26	0.37	0.46	0.55

- For $V_{GS} - V_{Th} << E_C L$, ($V_{GS} < 1V$) V_{DSat} is close to V_{GS}-V_{Th}
- For large V_{GS}, V_{DSat} would start bending upwards toward $E_C L$, but we won't even notice it with 1.2V supply.
- Therefore $E_C L$ can be frequently approximated with a constant term ($E_C L = 1.2V$ in 0.13µm)

Velocity Saturation



Drain Current

- We can also find the current

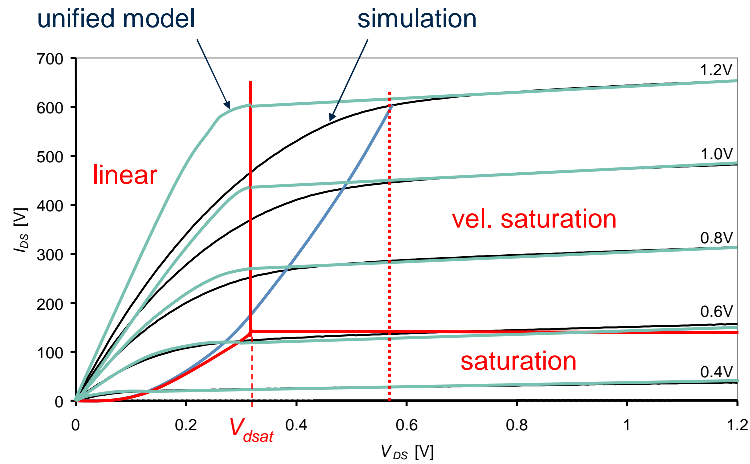
$$I_{DSat} = v_{Sat} W C_{ox} \frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_C L}$$

- Good model, could be used in hand or Matlab analysis

$$I_{DSat} = \frac{W}{L} \frac{\mu_{eff} C_{ox} E_C L}{2} \frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_C L}$$

$$I_{DSat} = \frac{W}{L} \frac{\mu_{eff} C_{ox}}{2} V_{DSat} (V_{GS} - V_{Th})$$

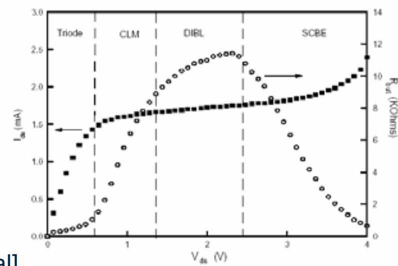
Drain Current



23

Output Resistance

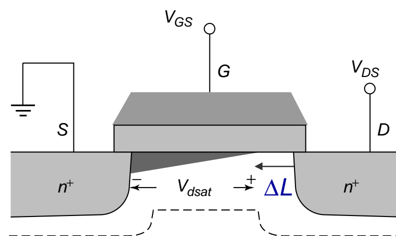
- **Slope in I-V characteristics caused by:**
  - Channel length modulation
  - Drain-induced barrier lowering (DIBL)
- **Both effects increase the saturation current beyond the saturation point**
- **The simulations show approximately linear dependence of I_{ds} on V_{ds} in saturation.**



[BSIM 3v3 Manual]

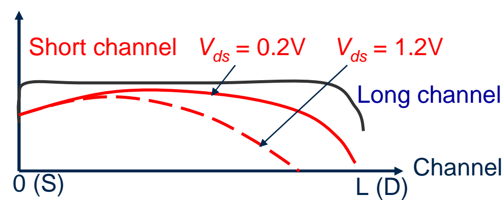
Output Resistance

- **Channel length modulation**
  - As the drain voltage increases beyond the saturation voltage V_{dsat}, the saturation point moves slightly closer to the source (ΔL)
  - The equation is modified by replacing L with ΔL
  - Taylor expansion $I_{ds} = I_{dsat}(1 + V_{ds}/V_A)$



Output Resistance

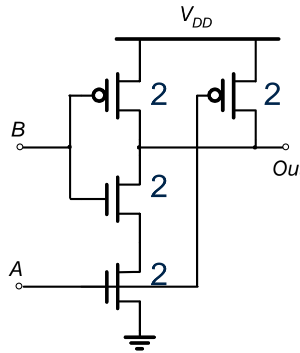
- **DIBL**
  - In a short channel device, source-drain distance is comparable to the depletion region widths, and the drain voltage can modulate the threshold
  - $V_{Th} = V_{Th} - \xi V_{ds}$
  - Taylor expansion



[Taur, Ning]

NAND GAte

- 2-input NAND gate

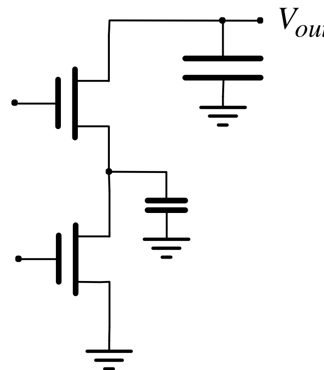


Sizing for equal transistions:
• P/N ratio (β-ratio) of 2 (more about this later in the class)
• Upsizing stacks by a factor proportional to the stack height

27

Transistor Stacks

- With transistor stacks, V_{DS}, V_{GS} reduce.
- Unified model assumes V_{DSat} = const.
- For a stack of two, appears that both have exactly double R_{ekv} of an inverter with the same width
- Therefore, doubling the size of each, should make the pull down R equivalent to an inverter



28

Velocity Saturation

- As $(V_{GS}-V_{Th})/E_CL$ changes, the depth of saturation changes

$$I_{DSat} = \frac{W}{L}\frac{\mu_{eff}C_{ox}E_CL}{2}\frac{(V_{GS}-V_{Th})^2}{(V_{GS}-V_{Th})+E_CL}$$

  - For V_{GS}, V_{DS} = 1.2V, E_CL is 1.3V
  - With double length, E_CL is 2.6V (in this model)
  - Stacked transistors are less saturated
  - $V_{GS}-V_{Th} = 0.95$V, I_{DSat} ~ 2/3 of inverter I_{DSat} (63%)
  - Therefore NAND2 should have pull down sized 1.5X
  - Check any library NAND2's

Velocity Saturation

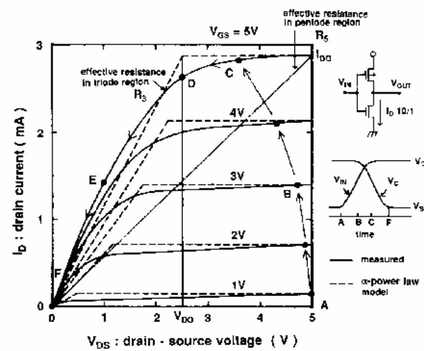
- How about NAND3?
- I_{DSat} = 1/2 of inverter I_{DSat} (instead of 1/3)
- How about PMOS networks?
- NOR2 – 1.8x, NOR3 – 2.4x, NOR4 - 3.2x
- What is E_CL for PMOS?

Alpha Power Law Model

- **Alternate approach, sometimes useful for hand analysis**

$$I_{DS} = \frac{W}{2L}\mu C_{ox}(V_{GS} - V_{Th})^{\alpha}$$

- Parameter α is between 1 and 2.
- In 0.13 - 0.25μm technology $\alpha \sim 1.2$.



[Sakurai, Newton, JSSC 4/90]

31

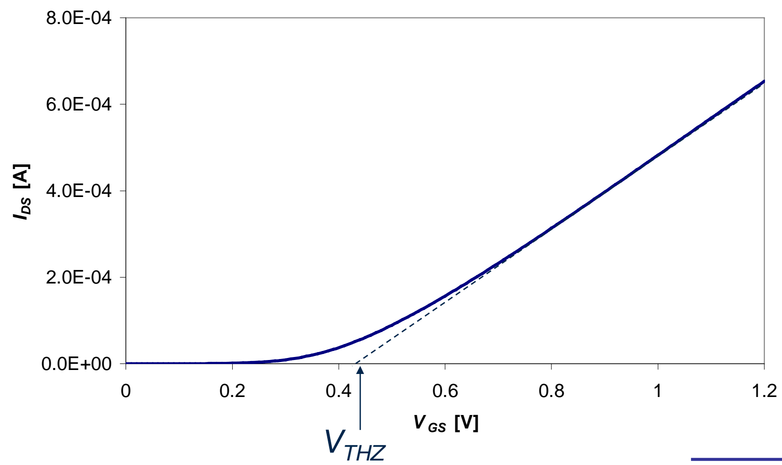
Alpha Power Law Model

- **This is not a physical model**
- **Simply empirical:**
  - Can fit (in minimum mean squares sense) to variety of α's, V_{Th}
  - Need to find one with minimum square error – fitted V_{Th} can be different from physical
  - Can also fit to α = 1
    - What is V_{Th}?

32

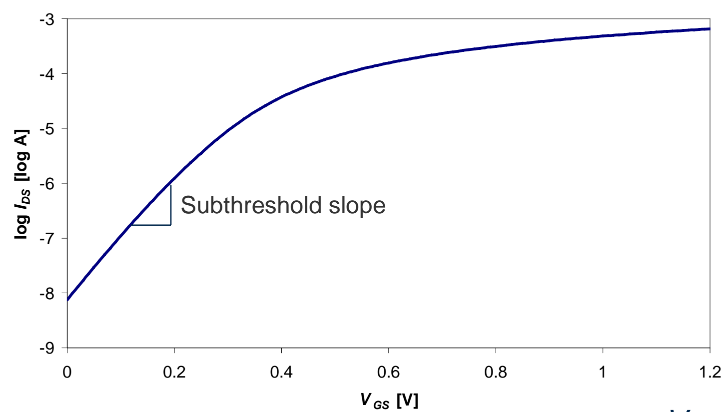
$K(V_{GS} - V_{THZ})$ Model

Drain current vs. gate-source voltage



33

Transistor Leakage

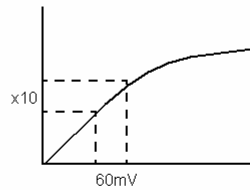


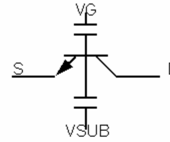
V_{DS} = 1.2V

Leakage current is exponential with V_{GS}

34

Transistor Leakage





slope factor S = kT/q ln10(1+ C_d/C_i)

kT/q 60mV/decade

C_d depletion layer cap

C_i gate oxide capacitance

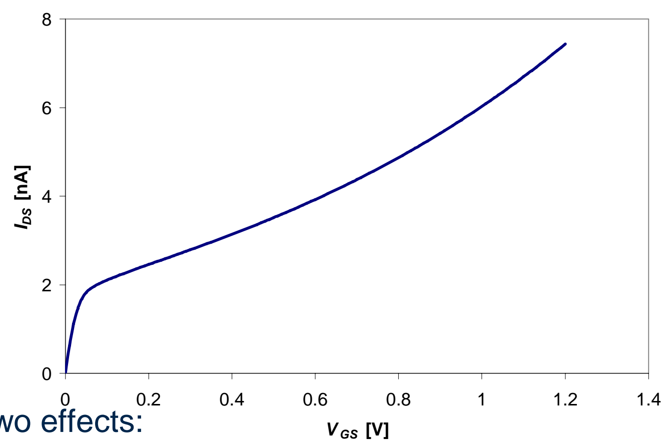
Typical value S ~ 70-90mV

V_T >> S

Solution: Newer device structures

Eg: thin film SOI transistors with fully depleted channels

Transistor Leakage



Two effects:

- diffusion current (like a bipolar transistor)
- exponential increase with V_{DS} (DIBL)

Subthreshold Current

- Subthreshold behavior can be modeled physically

$$I_{ds} = \mu \frac{W}{L} \left(\frac{kT}{q} \right)^2 e^{\frac{V_g - V_{Th}}{mkT/q}} \left(1 - e^{-\frac{Vds}{kT/q}} \right)$$

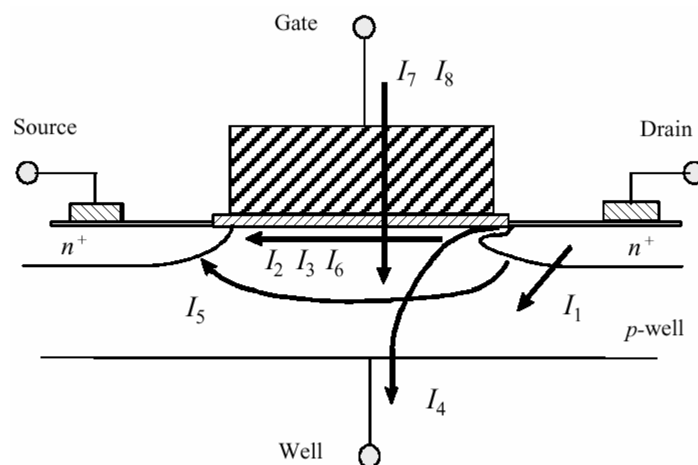
[Taur, Ning]

Or:

$$I_{ds} = I_0 \frac{W}{W_0} 10^{\frac{(V_{gs} - V_{Th}) + \gamma V_{ds}}{S}}$$

37

Leakage Components



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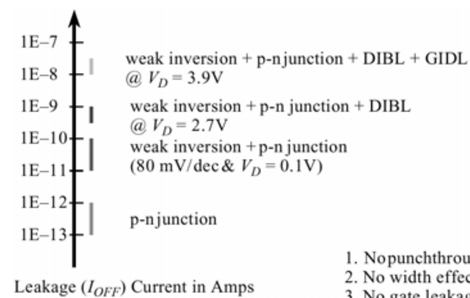
38

Leakage Components

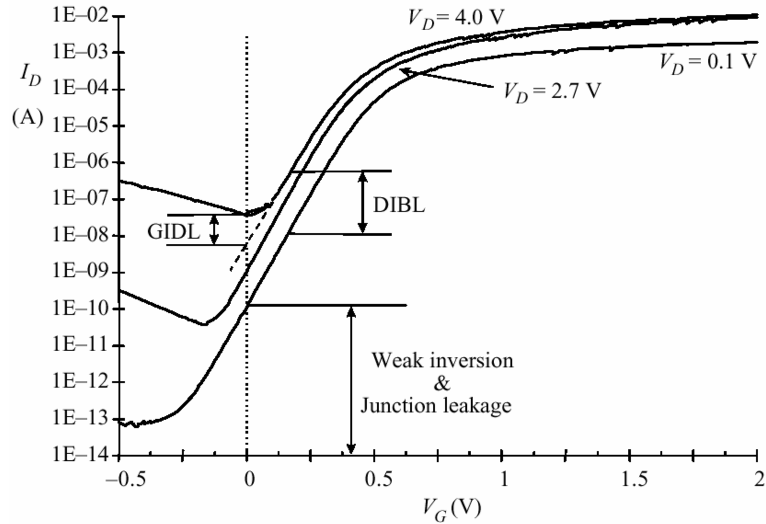
1. pn junction reverse bias current
2. Weak inversion
3. Drain-induced barrier lowering (DIBL)
4. Gate-induced drain leakage (GIDL)
5. Punchthrough
6. Narrow width effect
7. Gate oxide tunneling
8. Hot carrier injection



Leakage Components

- **Drain-induced barrier lowering (DIBL)**
  - Voltage at the drain lowers the source potential barrier
  - Lowers V_{Th}, no change on S
- **Gate-induced drain leakage (GIDL)**
  - High field between gate and drain increases injection of carriers into substrate -> leakage
    (band-to-band leakage)

DIBL, GIDL, Weak Inversion



41

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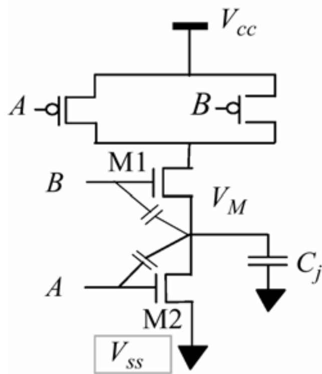
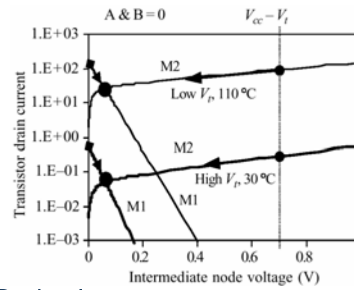
Stack Effect

NAND gate:





Reduction:

	High V_t	Low V_t
2 NMOS	10.7X	9.96X
3 NMOS	21.1X	18.8X
4 NMOS	31.5X	26.7X
2 PMOS	8.6X	7.9X
3 PMOS	16.1X	13.7X
4 PMOS	23.1X	18.7X

42

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