

Design Considerations for Logic Operating in the IC=1 Regime

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Abstract – Historically, most of the energy in digital circuit design has been focused on increasing the performance and computational power available by increasing density of devices and by increasing the frequency of operation. However, recent developments in fields such as wireless communication, which require not only good performance, but also an emphasis on low power and energy consumption, are changing the paradigms of digital circuit design. In this project, we aim to explore the possibilities of digital logic design in moderate inversion to take advantage of the same advantages afforded to analog circuits in this region. The project will first focus on establishing an adequate model of digital circuit performance in moderate inversion, which will be used to identify tradeoffs and optimization methods. This model will then be used to design a proof-of-concept circuit, which will be used to compare this region to strong inversion designs as well as deep sub-threshold (weak inversion) designs. The comparison will include energy and performance as well as effects of parameter variations due to process and temperature.

I. Introduction

Much research has been conducted on the use of moderate inversion in analog circuit design as a compromise between the low power consumption of weak inversion and the high speed of strong inversion. There has been a significant amount of research into methods of optimizing digital circuit design, such as [1-3], [5-6]; however, it has previously focused on either strong inversion operation or weak inversion operation. By including the moderate inversion region, which features significantly higher on currents than weak inversion while not increasing the V_{DD} significantly, we believe a substantial performance gain is possible while still retaining much of the low power benefits of weak inversion. We are planning to extend this work using a model valid for all regions of

operation to demonstrate the potential of operation in the moderate inversion regime.

To facilitate this, a model has been developed which is valid in all three modes of operation and accounts for modern device non-idealities such as DIBL. This model has been calibrated using SPICE simulations and shown to be accurate over the desired range. The details of this model will be discussed in section II, and a description of the proposed work for the remainder of the project will be given in section III.

II. Modeling Energy and Delay

Models for the most important performance measures for digital circuits, propagation delay (T_d) and energy per operation (EOP) were developed in order to compare the performance of logic operating in the region $IC=1$ (moderate inversion) to other regions of operation,

Similar to [1] and [2] the delay of a logic gate can be expressed as

$$T_d = \frac{C \cdot V_{DD} \cdot k_{fit}}{IC \cdot I_s} \quad (1)$$

where C is the load capacitance of the gate, k_{fit} is a fit factor and IC is the inversion coefficient defined by [4] as

$$IC = \frac{I_{DS}}{I_s} \quad (2)$$

with

$$I_s = 2 \cdot n \cdot \mu \cdot C_{OX} \cdot \frac{W}{L} \cdot U_T^2 \quad (3)$$

In equation (3), n represents the sub-threshold slope factor, μ the mobility, C_{OX} the oxide capacitance, W and L the width and the length of the transistor respectively, and U_T the thermal voltage

given by kT/q , which is approximately equal to 26mV at room temperature.

Assuming the transistors operate in saturation and V_{GS} is equal to V_{DD} , which is in general the case for static CMOS logic, V_{DD} can be expressed in terms of IC by

$$V_{DD} = \frac{V_T + 2nU_T \ln(e^{\sqrt{IC}} - 1)}{1 + \sigma} \quad (4)$$

with V_T being the threshold voltage and σ being the DIBL factor. Equation (4) was derived based on the transistor model for the drain current in and above weak inversion presented in [5], by replacing V_{GS} by V_{DD} and taking DIBL into account. The only remaining weak point of this model is that it does not take velocity saturation into account, which is acceptable for the purpose of this work since it is concerned mainly on relatively low values of V_{DD} .

The energy per operation can generally be expressed by

$$EOP = V_{DD} \cdot I_{leak} \cdot T_d \cdot L_p + \alpha \cdot V_{DD}^2 \cdot C \quad (5)$$

with I_{leak} being the leakage current, L_p the logic depth of the critical path and α being the switching activity factor [3]. The first term of equation (5) represents the energy consumption due to leakage and the second one the contribution of the dynamic switching power. This basic equation for the energy per operation neglects the energy due to the short circuit current flowing during the time when both transistors are on, since it only occurs for V_{DD} larger than V_T and is negligible for small values of V_{DD} .

For the leakage current I_{leak} the simple weak inversion transistor model of [4] was used, where V_{DD} was assumed to be significantly larger than U_T (at least 4x) and DIBL was taken into account additionally, leading to

$$I_{leak} = I_S \cdot e^{\frac{\sigma \cdot V_{DD} - V_T}{n \cdot U_T}} \quad (6)$$

By using the equations (1) to (6), both delay and energy can now be expressed in terms of IC .

The developed models were calibrated to the 90nm predictive models provided for this class, and a comparison between our model and simulation results are shown in Fig. 1 and Fig. 2 for propagation delay and energy per operation respectively. Both models show a very good match for almost the entire range of interest for IC , only the delay model starts deviating from the simulated delay for high values of IC .

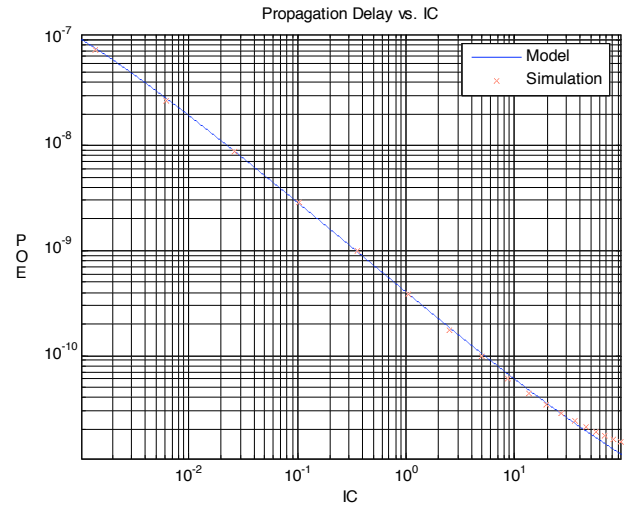


Figure 1. Propagation Delay vs. IC, simulation versus model

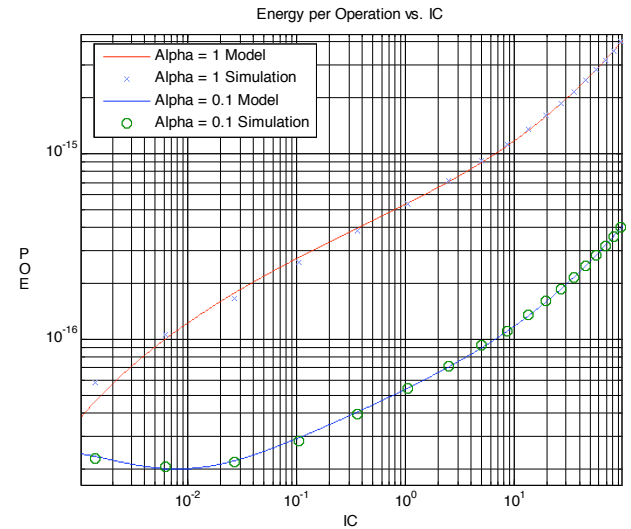


Figure 2. Energy per Operation vs. IC for different values of α , simulation versus model

The optimistic delay predicted by our model is due to the fact that it does not consider velocity saturation, which slows down the logic at high levels of V_{DD} , as shown by the simulation results in Fig. 1. Further, Fig. 2 provides the results for two different values of α , 1 and 0.1 respectively.

III. Proof-of-Concept Work

For the remainder of the project we plan to investigate the effect of parameter variations in the different regions of operation and to design a common datapath block, such as an adder, in order to analyze the benefits of operating in the moderate inversion region.

It is important to note here that we will be looking at different figures of merit during our design, known as ED^n [7]. This ensemble of figures of merit allows us to specify how important energy savings are versus delay penalties. For example, ED^1 represents the common energy-delay-product and means that a designer is willing to give up 1% in energy in order to increase speed by 1%. On the other hand, ED^2 means a designer is willing to give up 2% in energy in order to increase speed by 1%. Therefore, depending on the specific application, different values of n would be appropriate. Please note, however, that n does not have to be an integer greater than 1. If a fraction such as $\frac{1}{2}$ is used, it can be considered to be the inverse figure of merit of ED^2 , meaning that the designer is willing to give up 2% in speed in order to decrease energy by 1%.

In order to facilitate the design process, we will first develop an optimization approach using Matlab similar to the approach used in [6]. We will use the equations from section II to create a minimization problem in Matlab with parameters such as transistor sizing (W), supply voltage (V_{dd}), and threshold voltage (V_{th}). This will allow us to efficiently tune these parameters and observe their effects on the different figures of merit mentioned above and determine whether moderate inversion operation is highly beneficial for one figure of merit in particular. Further we hope to expand the

optimization approach of [6] throughout the different regions of operation in order to find a optimum design point for a given performance constraint independent of the region of operation.

Upon choosing an optimum operating point, we will implement the circuit in order to compare its performance with that predicted by our model.

Finally, we hope to show that there are certain cases where operating in moderate inversion region rather than in the more traditional strong inversion, or the extremely low power weak inversion region, is beneficial, and to identify the most important design considerations that come along with it.

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