



University of California  
College of Engineering  
Department of Electrical Engineering  
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ThFr, May 12-13, 2005.

## EE241—SPRING 2005: TAKE HOME FINAL

Due Fr May 13 at noon in 558 Cory.  
NO LATE SUBMISSIONS WILL BE ACCEPTED.

**ALSO: THIS IS A STRICTLY INDIVIDUAL  
EFFORT.**

<b>NAME</b>	Last	First
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<b>GRAD/UNDERGRAD</b>	
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**Problem 1:**

**Problem 2:**

**Problem 3:**

**Problem 4:**

**Problem 5:**

**Total:**

### PROBLEM 1. Scaling.

The path from data cache to register file of a microprocessor involves 500 ps of gate delay and 500 ps of wire delay along a repeated wire (that is, a wire with optimal repeaters). The chip is scaled using constant field scaling and reduced height wires with a scaling factor  $S = 2$ . Estimate the gate and wire delays of the scaled data path. By how much did the overall delay improve?

### PROBLEM 2. Low-voltage design.

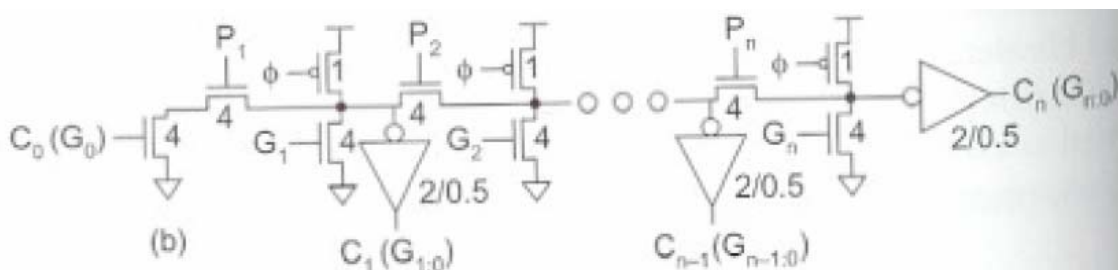
Read carefully the paper by Calhoun and Chandrakasan (attached), published at this years ISSCC conference. After that, address the following questions:

- Derive an expression for the normalized energy per operation versus rate for ideal DVS. Do the same for the voltage dithering approach using  $n$ -equally distributed supply voltages (assume operation above threshold for all voltages).
- Using the data from the paper, compute the energy savings over the fixed voltage (at 1.1V) for a scenario where 60% of the additions have no timing limit, 25% need to be performed at rate  $10^{-4}$  and 15% at rate  $10^{-1}$  for both the DVS and the UDVS approaches.

### PROBLEM 3: Adders and Logical Effort

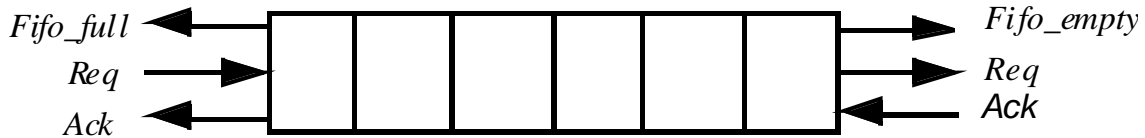
- Develop equations for the logical effort and parasitic delay with respect to the  $C_0$  input of an  $n$ -stage Manchester carry chain block computing  $C_1 \dots C_n$ . Consider all the internal diffusion capacitances when deriving the parasitic delay. Use the transistor widths shown in the Figure and assume the  $P_i$  and  $G_i$  transistors of each stage share a single diffusion contact.
- Using the results of a, what Manchester Carry Chain block length gives the least delay for a long adder.

PS Use symbolic values for the undefined variables.



#### PROBLEM 4. Self-Timed Circuits

Design a self-timed FIFO at the transistor level. It should be six stages deep and have a four-cycle interaction with the outside world. The black-box view of the FIFO is given in the Figure below.



#### PROBLEM 5. Synchronization

LousyCircuits, Inc., wants to sell you a perfect synchronizer that they claim never produces a metastable output. The synchronizer consists of a regular latch followed by a high-gain comparator that produces a high output for inputs above  $V_{DD}/4$  and a low output for inputs below that point. The VP of marketing argues that even if the flip-flop enters metastability, its output will hover near  $V_{DD}/2$  so the synchronizer produces a good high output after the comparator. Explain why you would not buy this synchronizer.