

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences
Last modified on April 25, 2002 by Jason Hu (hujas@bwrc.eecs.berkeley.edu)

Jan M. Rabaey
 Andrei Vladimirescu

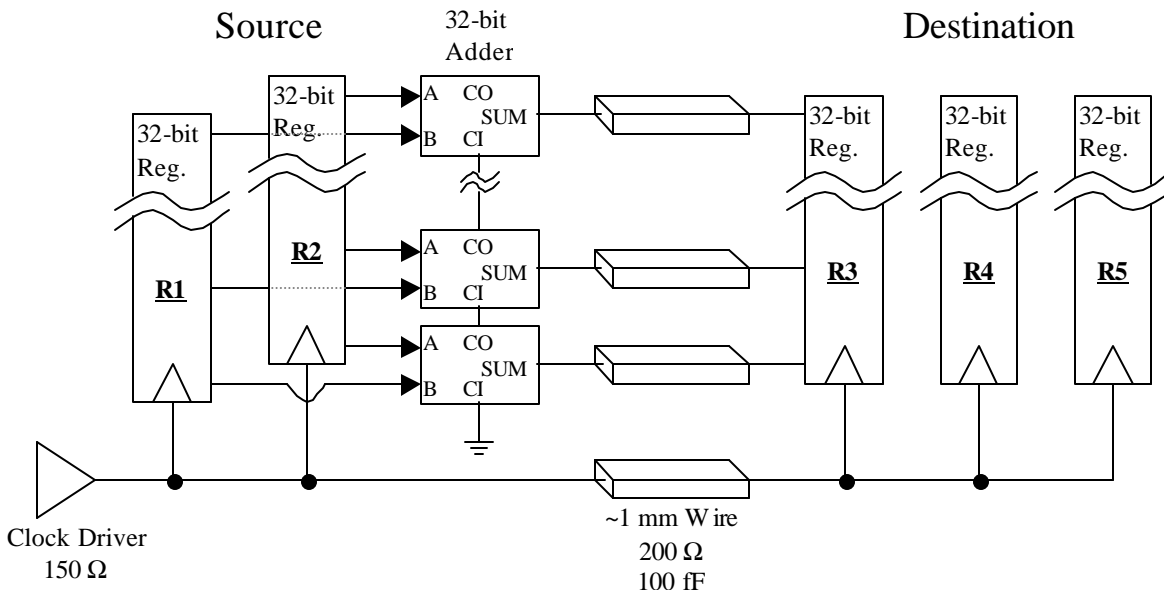
Homework #10
 Due Friday 5/10/02 5pm, 558 Cory

EECS 141

Problem 1 – Timing & Race Conditions

The following circuit consists of a source portion which adds the outputs of two registers R1 & R2 and a destination portions which stores the sum in R3. The connections between the source and the destination are made by an automatic router which creates wires with an average length of 1mm and containing an average of 10 contact holes in series. This leads to a resistance of about 200 Ω and capacitance of about 100 fF for each wire.

A clock driver buffers the clock signal at the source and is routed by the same tool to the destination, where it connects to R3 and two other registers (R4 & R5) which happen to be close by. Each register presents a load of 300 fF to the clock driver.



Assume the following timing values for the logic: $t_{\text{carry}} = 250$ ps, $t_{\text{sum}} = 300$ ps (including the wire load), $t_{\text{setup}} = 150$ ps, $t_{\text{hold}} = 100$ ps, $t_{\text{clk-Q}} = 50$ ps.

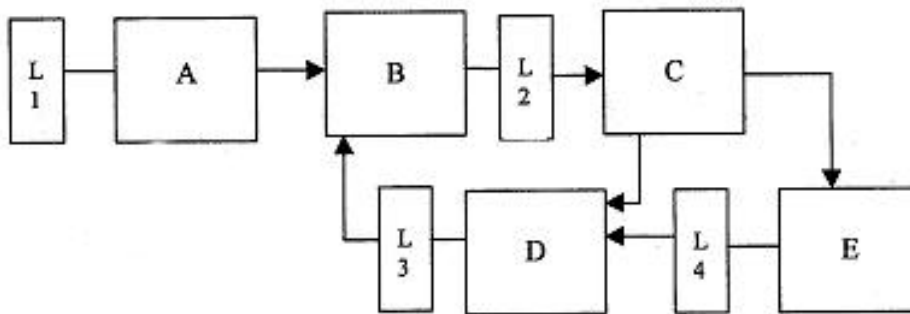
- Does this circuit have a race problem? What is the minimum clock period?
- What if you removed R4 and R5? Would there be a race problem? What would the new minimum clock period be?
- What if the driver were placed at the destination (with R3, R4 & R5)? Would there be a race problem? What would the new minimum clock period be?

Problem 2 – Timing and Clock Skew

- **Timing and Clock Skew**

3. (4pts) Logic Information. Assume all latches (1-4) are on the same clock and that the logic blocks are static.

$T_{\text{latch}} = 0.3\text{ns}$
 Block A: $T_{\text{min}} = 1\text{ns}$ $T_{\text{max}} = 2.1\text{ns}$
 Block B: $T_{\text{min}} = 1.7\text{ns}$ $T_{\text{max}} = 2.3\text{ns}$
 Block C: $T_{\text{min}} = 0.5\text{ns}$ $T_{\text{max}} = 1.4\text{ns}$
 Block D: $T_{\text{min}} = 2.2\text{ns}$ $T_{\text{max}} = 2.9\text{ns}$
 Block E: $T_{\text{min}} = 1.5\text{ns}$ $T_{\text{max}} = 3.1\text{ns}$



a.) Determine $T_{\text{ON,Max}}$, the maximum time that the clock pulse can be high (i.e. longest time the latches can be open for.) Assume there is NO clock skew.

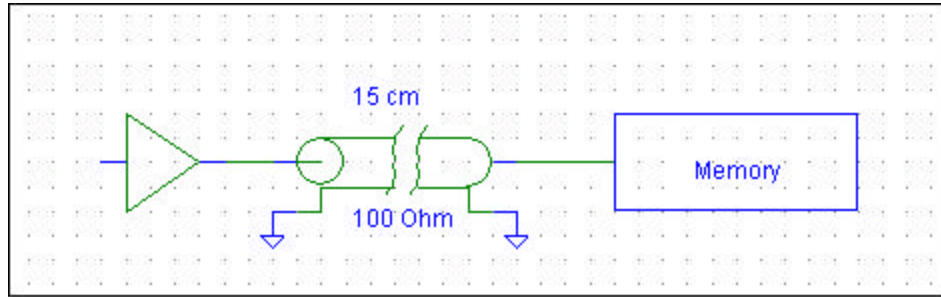
b.) Determine T_{Min} , the minimum clocking period. Once again, assume NO clock skew.

c.) Now assume that the clock is routed from latch 1 (L1) to latch 4 (L4) in ascending order. Assume that the clock skew between subsequent latches is the same (i.e. the skew from L1 to L2 is the same as the skew from L2 to L3). Find the MINIMUM clock skew needed to safely run the clock with a 4.5ns period. Ignoring the duty cycle of the clock for now, what is the MAXIMUM (if any) clock skew allowed such that we can still run the clock with a 4.5ns period?

d.) If the clock period is 5ns, what value of clock skew will safely allow the clock to be run at its maximum duty cycle? What is the maximum duty cycle under this condition?

e.) Now, assume that there is a latch (L5) added to the circuit between logic blocks A & B. Also assume that the clock is now routed to the latches in the following order: L1, L5, L2, L4, L3. If the latches are edge triggered, what are the constraints on the clock skew? (Assume no constraints on the clocking period and that the skew between latches is the same.) What is the minimum clock period that can be achieved?

Problem 3 – Transmission Line



To connect a processor to an external memory an off-chip connection is necessary. The copper wire on the board is 15 cm long and acts as a transmission line with a characteristic impedance of 100Ω . The memory input pins present a very high impedance which can be considered infinite. The bus driver is a CMOS inverter consisting of very large devices: (50/0.25) for the NMOS and (150/0.25) for the PMOS. The minimum size device, (0.25/0.25) for NMOS and (0.75/0.25) for PMOS, has the on resistance $35 \text{ k}\Omega$.

- Determine the time it takes for a change in the signal to propagate from source to destination (time of flight). The wire inductance per unit length equals $75 \cdot 10^{-8} \text{ H/m}$.
- Determine how long it will take the output signal to stay within 10% of its final value. You can model the driver as a voltage source with the driving device acting as a series resistance. Assume a supply and step voltage of 2.5V. Hint: draw the lattice diagram for the transmission line.
- Resize the dimensions of the driver to minimize the total delay.