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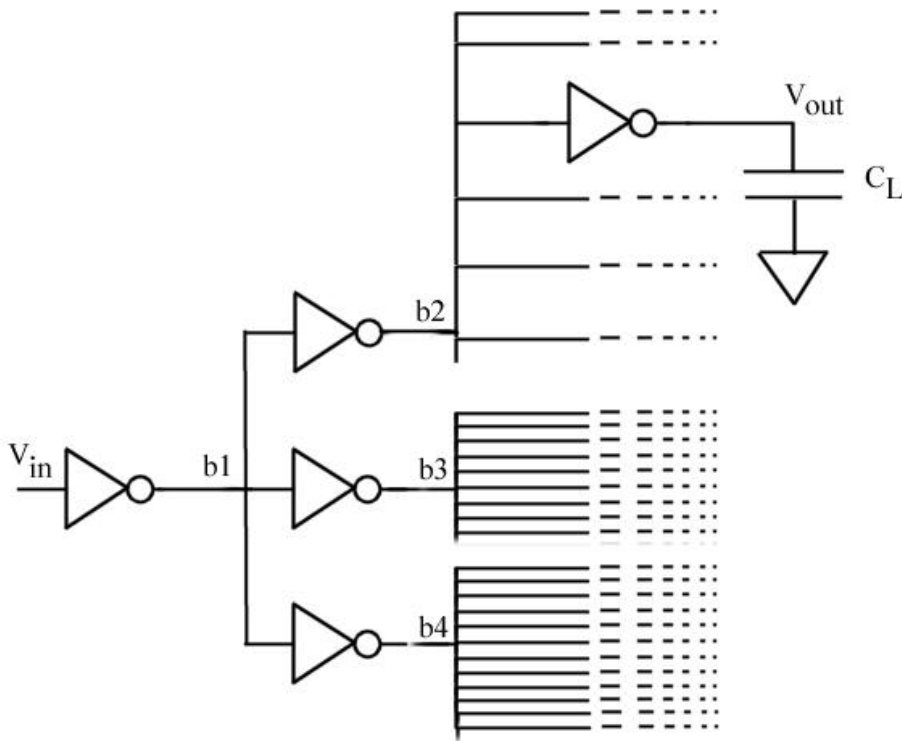
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*EECS 141*

*Homework #4: Delay, Capacitance, Power*  
*Due 2/20/02 at 5pm, 558 Cory*

**Problem #1: Propagation Delay**

Consider a clock network composed of inverters where each stage fans out to more inverters. There are a total of three stages:



**Figure 1: Clock Network**

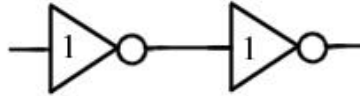
- At node b1, fan out is 3 inverters
- At node b2, fan out is 6 inverters
- At node b3, fan out is 9 inverters
- At node b4, fan out is 12 inverters

There is a load capacitor at the output of every inverter in the final stage. Given that the input capacitance of a minimum sized inverters is  $C_{in}$ , the output capacitor  $C_L$  is defined as  $96 C_{in}$ . Assume that  $V_{in}$  will be driven by a perfect step voltage.

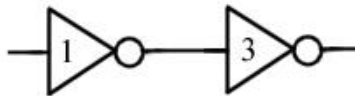
- a) First, we have to derive the important technology parameters that are essential in our propagation delay analysis. In the text, we derived the following expression for the delay:

$$t_p = t_{p\text{intrinsic}} + t_{p\text{load}} = t_{po} \left(1 + \frac{f}{g}\right)$$

We will determine the parameters of this equation through measurements on two test circuits. For the first circuit, a delay of a chain of two minimum sized inverter, we obtain that  $t_{p1} = 5 \text{ ns}$ .



The delay of a chain of two inverters where the first is minimum sized and the second one is 3 times minimum, equals  $t_{p2} = 7 \text{ ns}$ .

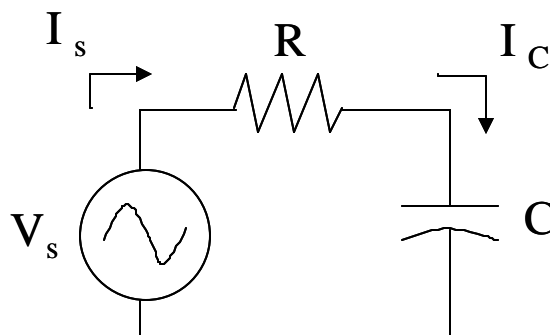


Using this information, calculate  $t_{po}$  and  $\gamma$ .

- Given that the first stage is minimum sized, size the inverters at the remaining two stages such that the propagation delay between  $V_{in}$  and  $V_{out}$  is minimized.
- Using the values you calculated in part a, and if the inverters are sized as described in part b, what would be the propagation delay of the first stage? The second stage? The third stage? The total delay?

**Problem #2: Adiabatic capacitor charging**

Adiabatic charging is a method used to reduce energy dissipation in a system. Typically, this technique is used to reduce dissipation when charging high capacitance loads or loads that require high voltages. We will calculate the energy dissipation of a simple RC circuit given three different types of charging sources.



**Figure 2: Simple RC circuit**

The energy dissipation in an RC circuit is dissipated by the resistor. There are a two ways to calculate the energy dissipation. The first is to calculate the energy drawn by the voltage supply and subtracting the energy delivered to the capacitor. The remaining energy would be the energy dissipated by the resistor.

The energy being drawn from the voltage supply is:

$$E_s = \int_0^{\infty} V_s(t) I_s(t) dt$$

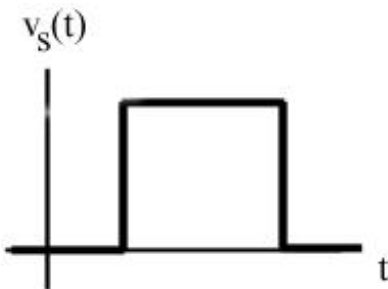
The energy delivered to the capacitor is:

$$E_c = \int_0^{\infty} V_c(t) I_c(t) dt$$

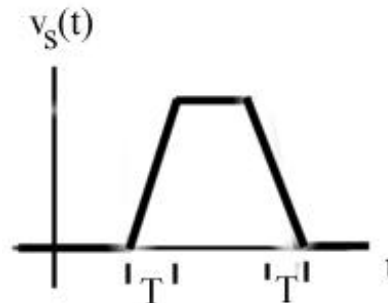
Alternatively, the energy dissipated can be calculated directly from the R by using the equation:

$$E_{diss} = \int_0^{\infty} I_s^2(t) R dt$$

**a) Single Step Input**



**b) Ramp Input**



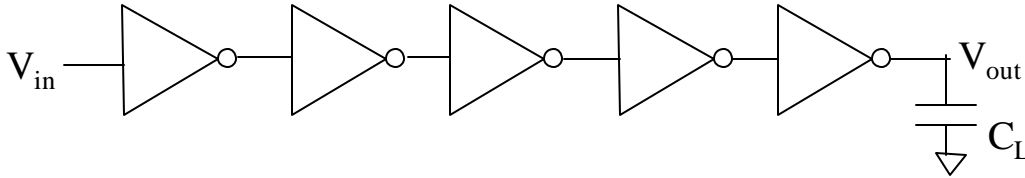
**c) Multi Step Input**



- Calculate the energy dissipation of one complete cycle of charging and discharging by a **single-step input**. Assume that there is sufficient time for the capacitor to fully charge before the start of the discharging.
- Calculate the total energy dissipation for a **ramp input**. Assume that it takes time T for the power supply to rise to  $V_s$ , and another time T for the power supply to decrease to zero. As time T is increased, what happens to your energy dissipation?

- c) Calculate the energy dissipation for **an N step input**. Again, assume that there is sufficient time for the capacitor to fully charge or discharge between each step, and that the steps are evenly distributed between 0 and  $V_S$ .
- d) What happens to the energy dissipation as N approaches infinity? Why is that?

**Problem #3: Sizing and Power**



**Figure 3: Inverter Chain**

$R = 50 \text{ k}\Omega$ ,  $C_{in} = 10 \text{ fF}$ ,  $C_{intrinsic} = 5 \text{ fF}$  (these are the values for minimum sized devices)

In this problem, we will study how sizing affects power consumption. Assume that we have a chain of 5 inverters and that we want to drive a capacitive load. The capacitive load is  $3.125 \text{ pF}$ . Assume that the above stated resistance and capacitances are for minimum-sized inverters. Our goal is to minimize our power consumption yet still have a delay less than  $30 \text{ ns}$ .

Power consumption is typically proportional to capacitance and voltage supply squared. For this particular problem, we will define power consumption as:

$$P_{tot} = C_{tot} V_{supp}^2$$

Assume that capacitance increases linearly with the size when calculating the total capacitance.

Decreasing the voltage supply on a circuit will increase the propagation delay by some factor. For our problem, we will simplify this and assume that propagation delay is inversely proportional to the supply voltage. Since we use  $V_{DD}$  as the baseline voltage, the delay will be:

$$t_{pVSUPP} = \left( \frac{V_{DD}}{V_{SUPP}} \right) t_{pVDD}$$

where  $t_{pVDD}$  is the propagation delay at  $V_{DD}$  and  $t_{pVSUPP}$  is the propagation delay at the alternative voltage. There are three different supply voltages that we can use:  $V_{DD}$ ,  $V_{DD}/2$ , and  $V_{DD}/3$ , where  $V_{DD} = 2.5\text{V}$ .

The question is, which supply voltage and sizing combination will result in the least power consumption, yet still have a delay that falls within the constraint?