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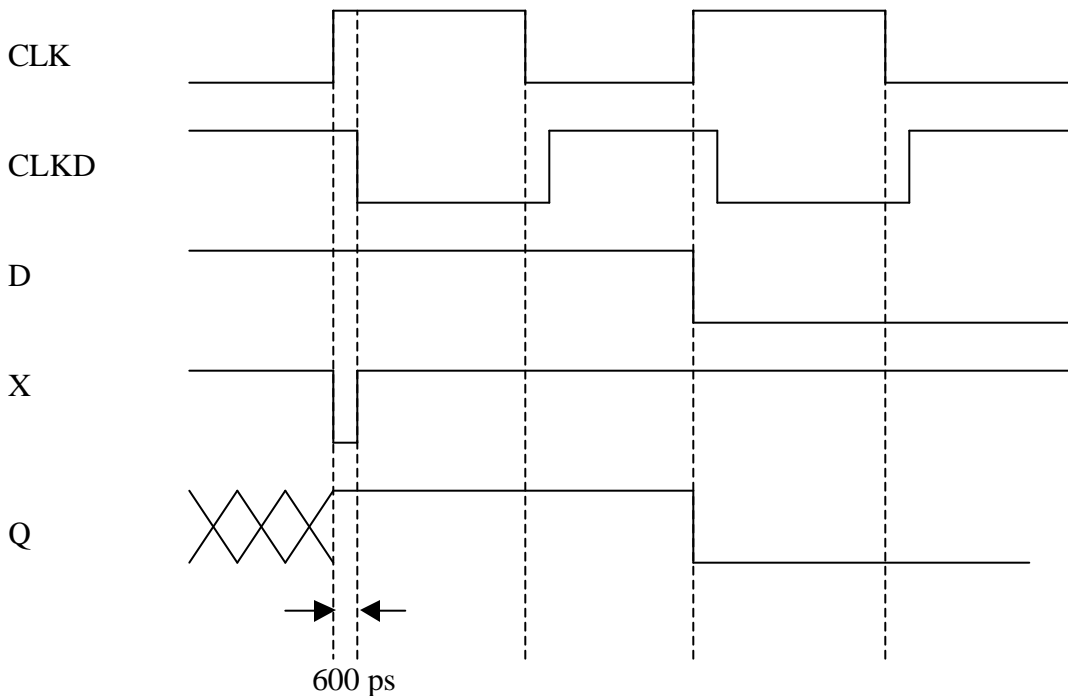
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**Homework #9 Solutions**

*EECS 141*  
*Spring 2003*

**Problem 1 – Pulse-triggered latch**

a)



b) With respect to clock rising edge,

$$\begin{aligned} t_{\text{setup}} &= 0 \\ t_{\text{hold}} &= 3 t_{p,\text{inv}} = 600\text{ps} \end{aligned}$$

c) There is only dynamic power consumption in this circuit.

$$\begin{aligned} P &= C V_{dd}^2 f_{0 \rightarrow 1} = (C_Q + C_{\bar{Q}}) V_{dd}^2 f_{CLK} 0.5 + C_X V_{dd}^2 f_{CLK} 0.5 + C_{CLKD} V_{dd}^2 f_{CLK} \\ &= (20f + 20f)(2.5)^2(100M) \times 0.5 \times 0.3 + 10f \times (2.5)^2(100M) \times 0.5 + 10f \times (2.5)^2(100M) = 13.1\text{mW} \end{aligned}$$

$$P = 13.1 \mu\text{W}$$

The red sign above indicates some correction to the original solution. The 0 to 1 switching probability is 0.5a for nodes Q and Q bar, while the same probability is 0.5 for node X, because X is precharged to  $V_{dd}$  before each clock rising edge. The 0 to 1 transition of X is only determined by the logical value of D at each clock rising edge, and is not affected by the probability (a) input D changes its state in the clock cycle.

## Problem 2 – Timing and Clock Skew

a) To determine the max. period that we can clock this system, we need to examine every possible path between the synchronous latches and the associated delay.

	Min	Max
L1→L2 passes through A, B	1ns+1.7ns=2.7ns	2.1ns+2.3ns=4.4ns
L2→L3 passes through C, D	0.5ns+2.2ns=2.7ns	1.4ns+2.9ns=4.3ns
L2→L4 passes through C, E	0.5ns+1.5ns=2.0ns	1.4ns+3.1ns=4.5ns
L4→L3 passes through D	2.2ns	2.9ns
L3→L2 passes through B	1.7ns	2.3ns

We want to focus on the minimum delay, because it is this factor which has the potential to through our system into a race condition. We see that the shortest combinational path is 1.7ns from L3→L2. Since there is also a .3ns  $t_{latch}$ . Thus our  $T_{on}$  must be within  $1.7ns+.3ns=2.0ns$

$$T_{on,max} = 2.0ns$$

b) For the Min. Period that we can clock the system we need to look at the max time:  $T_{min} = \max(\text{comb. Logic}) + t_{latch} = 4.5ns+.3ns = 4.8ns$  (note: if there were a setup time specified, we would have to take that into account)

$$T_{Pmin} = 4.8ns$$

c) Delay = ? (Block Delay) +  $T_{latch}$

Source Latch	Destination Latch	Min Delay ( $T_{min}$ )	Max Delay ( $T_{max}$ )	Skew	Race Constraint ( $T_{min} > \delta + T_{on}$ )	Clock Constraint ( $T_{max} < T_P + \delta$ )
L1	L2	3.0	4.7	$\delta$	$\delta < 3.0 - T_{on}$	$T_P > 4.7 - \delta$
L2	L3	3.0	4.6	$\delta$	$\delta < 3.0 - T_{on}$	$T_P > 4.6 - \delta$
L2	L4	2.3	4.8	$2\delta$	$\delta < (2.3 - T_{on})/2$	$T_P > 4.8 - 2\delta$
L4	L3	2.5	3.2	$-\delta$	$\delta > -2.5 + T_{on}$	$T_P > 3.2 + \delta$
L3	L2	2.0	2.6	$-\delta$	$\delta > -2.0 + T_{on}$	$T_P > 2.6 + \delta$

Concerns related to  $T_{on}$  is ignored in this problem. Thus,

For min  $\delta$ , consider L1→L2 case:

$$\delta > 4.7 - T_P = 0.2ns$$

For max  $\delta$ , Consider L4→L3 case:

$$\delta < 4.5 - 3.2 = 1.3 ns$$

c) Note that with  $T_P = 5.0ns$ , there is no longer a minimum skew requirement. From the race constraint column, can see that limiting case is set by L2 -> L4 and L3->L2

$$T_{on} < 2.3 - 2\delta$$

$$T_{on} < \delta + 2.0$$

To find the max.  $T_{on}$ , set  $2.3 - 2\delta = 2.0 + \delta \implies \delta = 0.1ns$

$$T_{on,max} = 2.1ns$$

$$\text{Duty Cycle} = 2.1/5.0 = 42\%$$

e)

Source Latch	Destination Latch	Min Delay ( $T_{min}$ )	Max Delay ( $T_{max}$ )	Skew	Race Constraint ( $T_{min} > \delta + T_{on}$ )	Clock Constraint ( $T_{max} < T_P + \delta$ )
L1	L5	1.3	2.4	$\delta$	$\delta < 1.3$	$T_P > 2.4 - \delta$
L5	L2	2.0	2.6	$\delta$	$\delta < 2.0$	$T_P > 2.6 - \delta$
L2	L3	3.0	4.6	$\delta$	$\delta < 3.0$	$T_P > 4.6 - \delta$
L2	L4	2.3	4.8	$2\delta$	$\delta < 2.3/2$	$T_P > 4.8 - 2\delta$
L4	L3	2.5	3.2	$-\delta$	$\delta > -2.5$	$T_P > 3.2 + \delta$
L3	L2	2.0	2.6	$-\delta$	$\delta > -2.0$	$T_P > 2.6 + \delta$

With no constraints on  $T_P$ , the max. skew is defined by propagation from L2->L4:  $\delta < 1.15$

For  $T_{P,min}$ , since that L2->L4 and L4->L3 have opposing behavior,

$$\text{Set } 4.8 - 2\delta = 3.2 + \delta \rightarrow \delta = 0.53ns$$

$$T_{P,min} = 3.73ns$$

### Problem 3 – Schmitt Trigger

a) When out is high, M6 is on providing a resistive path to Vdd, which makes it more difficult to bring the node between M3 and M4 low. When out is low, M5 is on providing a resistive path to ground, which makes it more difficult to bring the node between M1 and M2 high. This input-dependent switching threshold defines the circuit as a Schmitt trigger.

b) To prevent false-switch during both inputs, we need

$$V_{M+} > 1.5V, V_{M-} < 1V$$

c) Given that  $k_{p,NMOS} = 2.5 * k_{p,PMOS}$ , we size the PFETS, M1 and M2 to have 2.5 times the width of M3 and M4. We'll use 1um as the widths of M3 and M4. Then, without the presence of M5 and M6, we have a standard inverter with  $V_m = V_{dd}/2 = 1.25V$ .

Label the point where M6, M3 and M4 intersect to be called  $V_b$ . To have  $V_{M+}$  at 1.5V, we want M3 to turn on when  $V_{in} = 1.5V$ . This means that we want  $V_b$  to be 0.8V ( $V_{in} - V_T$ ). To set up  $V_b$  to be 0.8V, we need to size M6 versus M4 to create the right voltage division:  $0.8V = (V_{dd} * (R_4 / (R_4 + R_6)))$ . Let  $W_{M6} = X * W_{M4}$ . Assuming both transistors are in saturation, we have  $R = 1 / [\lambda * (k_p / 2 * (W/L) * (V_{GS} - V_T)^2)]$ . At the operating point under consideration,  $V_{GS4} = V_{in} = 1.5V$ , and  $V_{GS6} = V_{OUT} - V_b = 2.5 - 0.8 = 1.7V$ . Substituting into the voltage divider equation, we get  $X = 0.3$ . We also notice that in the voltage divider equation,  $\lambda$  and  $K_p$

get factored out. So the ratio of M4 to M6 is not dependent on these parameters. Therefore,  $W_{M6}/W_{M4}=W_{M5}/W_{M1}=0.3$ .

$$W_{M1} = W_{M2} = 2.5\mu\text{m}, W_{M3} = W_{M4} = 1\mu\text{m}, W_{M6} = 0.3\mu\text{m}, W_{M5} = 0.75\mu\text{m}$$

*Note: This solution treats serial transistors as voltage divider for simplicity. You can also solve current equations on the conducting path for results.*

d) The SPICE input deck and the simulation results are as following:

```
-----  
.model pmos pmos LEVEL=1 TOX=25 VTO=-0.7 KP=8e-6 LAMBDA=0.19 PHI=0.6  
.model nmos nmos LEVEL=1 TOX=25 VTO=0.7 KP=20e-6 LAMBDA=0.06 PHI=0.6  
.param wex=0.3  
  
M1 a in vdd vdd PMOS l=0.25u w=2.5u  
M2 out in a vdd PMOS l=0.25u w=2.5u  
M3 out in b 0 NMOS l=0.25u w=1u  
M4 b in 0 0 NMOS l=0.25u w=1u  
M5 a out 0 vdd PMOS l=0.25u w=`2.5u*wex`  
M6 b out vdd 0 NMOS l=0.25u w=`1u*wex`  
  
vdd vdd 0 2.5  
vin in 0 pulse 0 2.5 2ns 20ns 20ns 50ns 100ns  
  
.OPTIONS post=2 nomod  
  
.tran 1n 200ns  
.end  
-----
```

