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Homework #3

EECS 141

Due Thu., February 13<sup>th</sup>, 5pm @ 558 Cory

**Problem 1 – Inverter Delay Calculation**

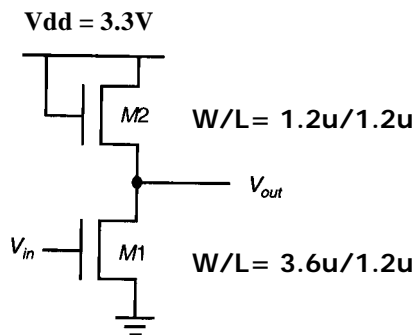
We have visited the two inverters shown below in homework 2. This time we are going to compare them on the performance metric. Assume that both of them are driven by a standard inverter (the high input voltage is  $V_{dd}$  and low input voltage is 0). There is a capacitive load  $C_L = 150\text{fF}$  on the output node of each inverter, which is large compared to the parasitic capacitances of the devices. **Use the same process parameters as in homework 2.**

**1A** For inverter A, prove that when the output voltage characteristics satisfy the following relation:  $V_M \approx (V_{OH} + V_{OL})/2$ , the delay for output to rise from  $V_{OL}$  to  $V_M$  (or fall from  $V_{OH}$  to  $V_M$ ) can be modeled as  $t_p = 0.69R_{eq}C_L$ , even if the output swing is not rail – to – rail. Here  $R_{eq}$  is the equivalent resistance of the device driving the output, and  $C_L$  is the load capacitance on the output node.

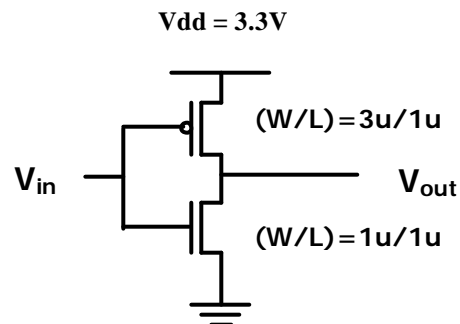
**1B** Evaluate the propagation delays of the two inverters using the VTC data we attained from last homework’s analysis. Here measure the delay of each inverter as the time between  $V_{IN} = V_M$  and  $V_{OUT} = V_M$ . Use the switch approximation analysis of the MOS transistor presented in class ( $R_{eq} = (R_M + R_{VOH}) / 2$ ) to estimate  $t_{pLH}$ , and same for  $t_{pHL}$ .

**1C** Verify  $t_{pLH}$  and  $t_{pHL}$  using HSPICE. (Note that there may be slight difference between your SPICE and hand calculation results, because approximations are used in our hand analysis. You can think about the reason for the discrepancy while you are not required to do so in this homework.)

**1D** Explain why M2 is sized to be much smaller than M1 in the first (all-NMOS) circuit? Briefly comment on that. What disadvantages on performance does the inverter with NMOS-load have compared to the CMOS inverter?



**Inverter A**



**Inverter B**

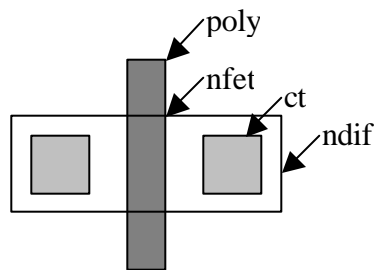
## Problem 2 – Computing the MOSFET Capacitances

**2A** It is always good to get a feel for design rules in a layout editor. Fire up **max** with the mmi25 (0.25  $\mu\text{m}$ ) technology file (this is the default setup). Place a minimum sized NMOS transistor and examine the dimensions. The layers are listed and shown below. Determine and list the following:

- Minimum Transistor Length
- Minimum Transistor Width
- Minimum Source/Drain Area

Please list the design rules you come across that lead to your results.

*TIPS - Use Shift-G to access the grid menu. Set the coarse grid to 0.1 $\mu\text{m}$ , fine grid to 0.01 $\mu\text{m}$   
Use Shift-Y to explain the design rules within a selected area*



**2B** We desire a minimum sized CMOS inverter with a symmetrical VTC ( $V_M = V_{DD}/2$ ) in the mmi25 technology. Calculate the desired size for the pull-up PMOS transistor, with the NMOS transistor minimum sized as in 2A.

- PMOS Transistor Length
- PMOS Transistor Width
- PMOS Source/Drain Area

Assume the following:

$V_{DD} = 2.5\text{V}$ ,  $V_M = 1.25\text{V}$ , use data in Table 3-2 in the textbook

**2C** Using the minimum size inverter from 2B, determine the input capacitance (i.e. the load it presents when driven), which is the total load capacitance that the inverter presents. Please calculate the capacitance during a transition. Use data in Table 3-5 in the textbook  
*\*Hint: Consider the Miller effect*

**2D** Using the same g25 model as you worked with in homework 2, verify your results in part c by determining the total input capacitance in a high-low and a low-high transition with HSPICE and comparing with your total capacitance in part c.

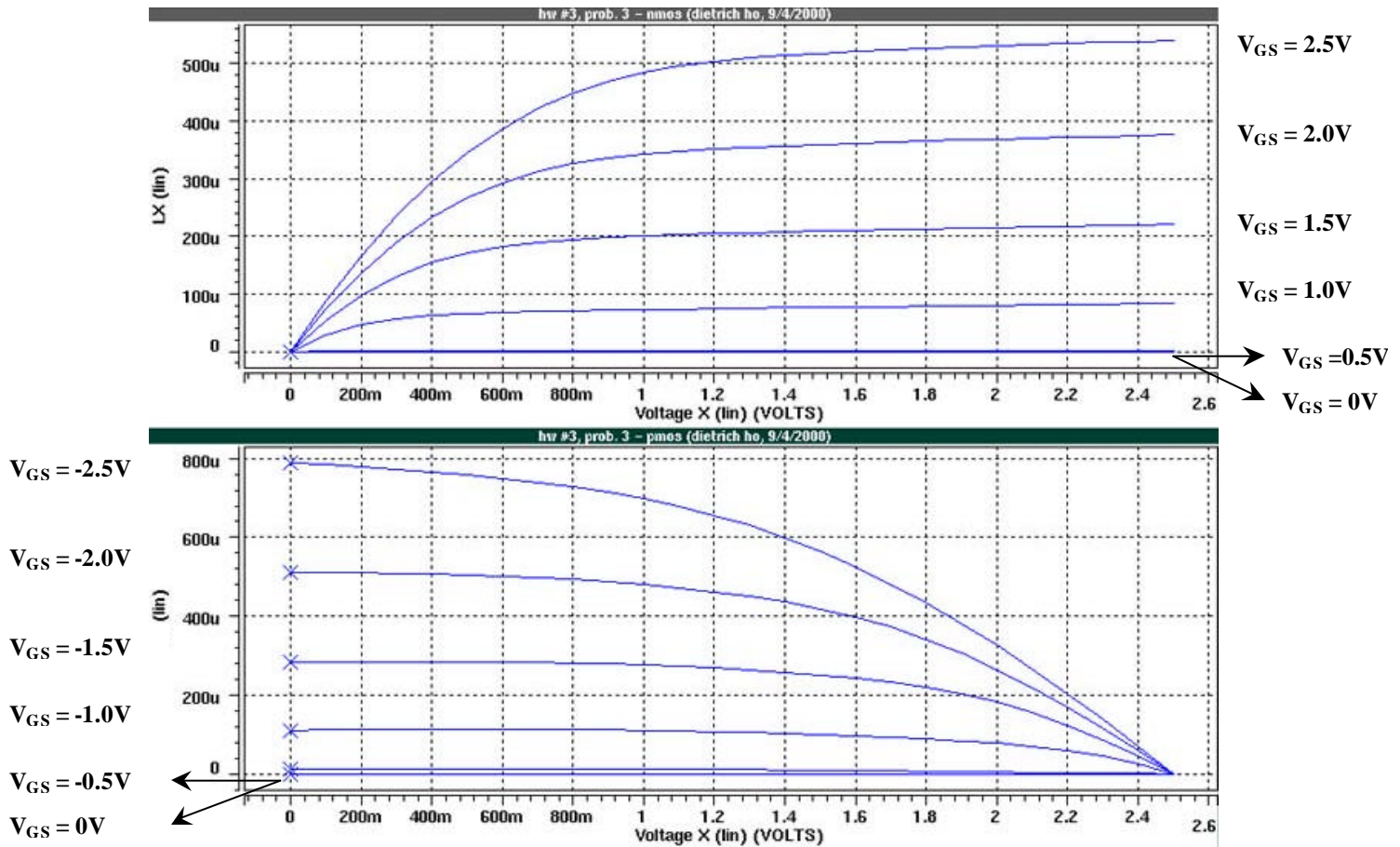
**2E** Determine  $V_{IH}$ ,  $V_{IL}$ ,  $NM_H$ , and  $NM_L$ .

*\*Hint: The 2 parameters  $r$  and  $g$  vary proportionally with transistor width. The equations given are derived with the minimum width in mind. (Please refer to Eq's 5.3 and 5.10 in the textbook for  $r$  and  $g$ )*

### Problem 3 – VTC of Inverter

- 3A** Figure 3a depicts the  $I_D - V_{OUT}$  curve of a typical NMOS transistor  
 Figure 3b depicts the  $I_D - V_{OUT}$  curve of a typical PMOS transistor

Assume we use these FETs to create a CMOS inverter. Using this family of curves, graph the VTC, and calculate  $V_M$ ,  $V_{IL}$ , and  $V_{IH}$ .



Top: Figure 3a, Bottom: Figure 3b

- 3B** If we increase the W/L ratio of the pull-down NMOS (leaving the PMOS size fixed), in which direction will the VTC shift?
- 3C** If instead, we increase the W/L ratio of the pull-up PMOS (and leave the NMOS the original size), in which direction will the VTC shift?
- 3D** Please explain how the resizing in 3B and 3C will affect the above I-V curves in each case and give an intuitive explanation of how this affects the VTC of each.