

HOMEWORK 1.**Due: Monday, February 21, 2000 at 5pm in 558 Cory****This is an individual assignment!****1. Spice models**

Use the BSIM3v3 (HSPICE Level 49, PSPICE Level 7) model to characterize a 0.25 micron CMOS process (TSMC); parameter files are on the class home page.

- a) Determine the threshold voltage V_T , for the NMOS and PMOS devices (for $V_{BS}=0$, $L = 0.25\mu\text{m}$ and $W = 1\mu\text{m}$), by extrapolating from the $I-V_{gs}$ curve at low V_{ds} . Determine also the body-effect parameter.
- b) Determine the subthreshold slope factor S for the NMOS and PMOS devices (at $V_{DS} = 2.5\text{V}$, room temperature). Determine the leakage currents at $V_{GS} = 0\text{V}$. Repeat it at a lower temperature $T=77\text{K}$.
- c) Determine the effects of channel length L on the threshold voltage V_T between $0.25\mu\text{m}$ to $2.0\mu\text{m}$. Draw V_T of the NMOS and PMOS as a function of L (for $V_{DS} = 2.5$ and 1.5V).
- d) Determine the effects of channel width W on the threshold voltage V_T between $0.5\mu\text{m}$ to $2.0\mu\text{m}$. Draw V_T of the NMOS and PMOS as a function of W (for $V_{DS} = 2.5$ and 1.5V).
- e) Determine the effects of drain-source voltage V_{DS} , on the threshold voltage V_T between 0 and 2.5 volts. Draw V_T as a function of V_{DS} (for $L = 0.25\mu\text{m}$).

2. Scaling

Explore the model for scaling a design from $0.35\mu\text{m}$ CMOS technology (supply 3.3V) to $0.25\mu\text{m}$ technology (supply 2.5V), using two TSMC models. Using the appropriate simulations predict the input capacitance, intrinsic propagation delay, and energy of an inverter ($W_n = 2L_{min}$, $W_p = 2W_n$) in two technologies and compare the results to generalized scaling theory.

3. Logical effort

Design a decoder for a 256-word register file, with each word being 32 bits wide, and each bit capacitance presenting one unit inverter load. Address lines are available as both true and complementary and may drive up to 2 unit inverter loads. Determine the optimum structure and sizing of the decoder for a minimum delay.

4. Design a CVSL gate with minimum number of transistors, implementing the logic function $F = ABC + \bar{A}B + AD$.