EE241 Advanced Digital Integrated Circuits **Spring 2000.**

HOMEWORK 2. **Due: Friday, March 3, 2000 at 5pm in 558 Cory**

This is an individual assignment!

1. Charge Sharing

a) Simulate the charge sharing in a dynamic CMOS gate from Figure 1.a, using Hspice and 0.25µm CMOS models. Assume that all the transistors have 1µm width and minimum length and that the output is loaded with an inverter (W(PMOS) = 2µm; W(NMOS) = 1µm). What is the voltage drop observed at the output node?

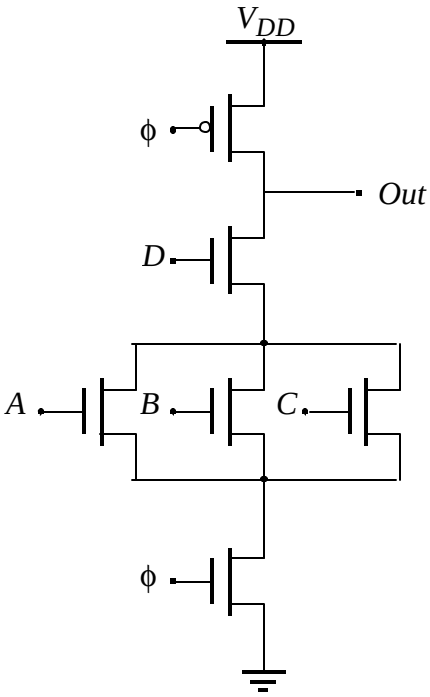

Figure 1.a

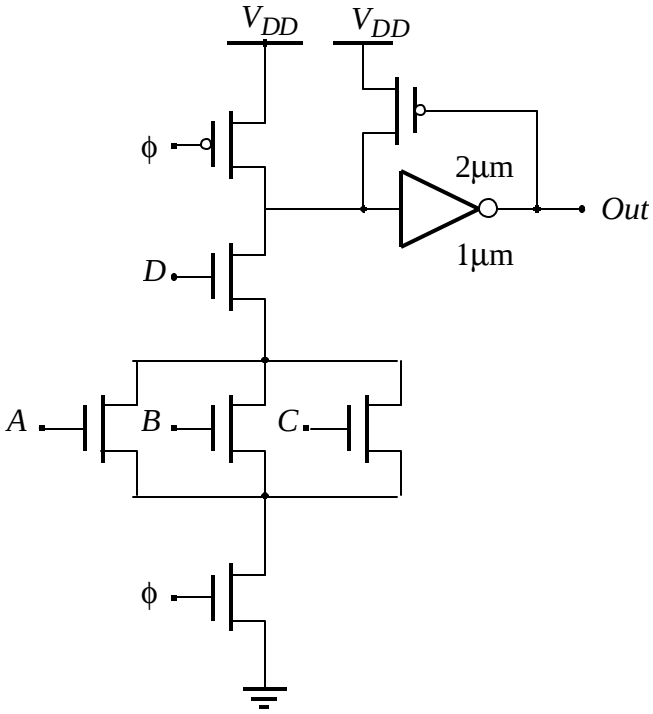

Figure 1.b.

b) Determine the impact on delay of the circuit from Figure 1.a. of:

- adding a static bleeder to the output node.
- precharging the internal node.

c) Show by simulation the sizing tradeoff of the keeper transistor from Figure 1.b (sizing of the dynamic gate is unchanged from Figure 1.a). Comment the observed results.

2. RC Delays

Use the parameters for TSMC 0.25µm model and assume Vdd=2.5V, V_{DSAT}=1V, neglect body effect.

a) Using the deep submicron transistor models for hand analysis, determine the equivalent resistance of the transmission gate as a function of terminal voltage, for both pull-up and pull-

down transitions. Plot the resistance as a function of terminal voltage. What is an equivalent average value of this resistance in 0.25µm process, as a function of Wp and Wn?

b) Using appropriate approximations for parasitic capacitances, how would you determine the optimum sizing between PMOS and NMOS transistors in the transmission gate, for 0.25µm process? Keep the NMOS transistor width fixed at 1µm, and determine the PMOS width that minimizes the delay in a chain of equivalent transmission gates.

c) What is the optimum value of chain length of these gates (with the sizing from part b.) before buffer insertion. What determines the size of the buffer?