

HOMEWORK 3.

Due: Tuesday, March 21, 2000 at 5pm in 558 Cory

This is an individual assignment!

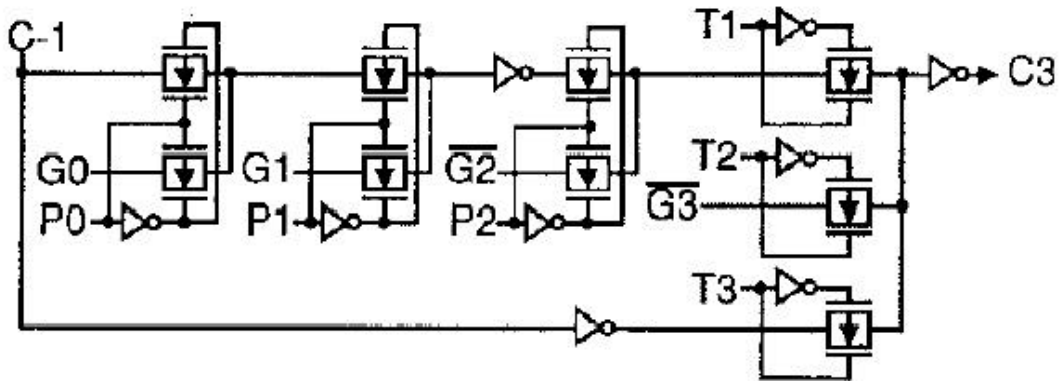
1. Conditional sum adder

- a) Find an error in a table that demonstrates conditional sum addition in slide 25, page 13 of lecture 16 notes.
- b) Demonstrate the conditional summation by a similar table for inputs $x = 10110110$ and $y = 00101101$.

2. Carry-skip adder

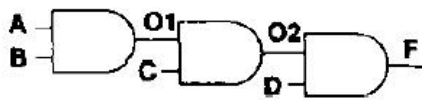
- a) Design a 16-bit carry skip adder with equal group lengths using standard, complementary CMOS gates. Use a full adder cell as a building block for ripple-carry groups.
- b) Assume that all gates have the same delays. Determine the optimal group length, k , as a function of adder length, n .

3. Another carry-skip adder

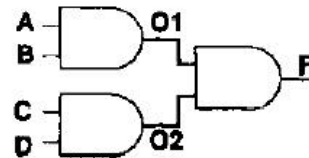


- a) A carry-skip group is shown in figure above. P_i and G_i are propagate and generate signals at bit positions i . $C-1$ and $C3$ are input and output carry signals. Briefly describe the operation of the circuit. What do you think is the reason for the difference in its logic design compared to the one shown in class? What would be the advantage of this approach?
- b) Derive the required signals $T1$, $T2$ and $T3$ as a function of signals P_i and G_i .

4. Switching Activities



Chain structure



Tree structure

Compute the switching probabilities of the output, F , and internal nodes $O1$ and $O2$, for the chain and tree implementations of 4-input AND gates, for the cases when input switching probabilities $(P(A) = P(B) = P(C) = P(D))$ equal a) 0.5; b) 0.25.