

## HOMEWORK 4.

Due: Tuesday, April 11, 2000 at 5pm in 558 Cory

**This is an individual assignment!**

1. **Transmission lines.** Assume  $V_{DD}=1.5V$ , using  $0.25\mu m$  class technology.

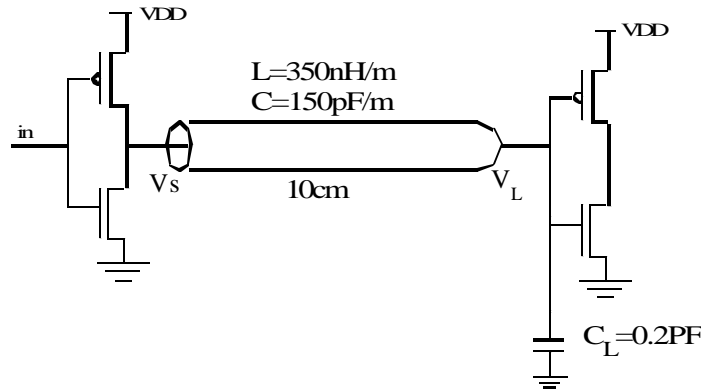


Figure 1: Transmission line.

- The Figure 1 shows an output driver feeding a 0.2 pF effective fan-out of CMOS gates through a transmission line. Size the two transistors of the driver to optimize the delay. Sketch waveforms of  $V_S$  and  $V_L$ , assuming a square wave input. Label critical voltages and times.
- Size down the transistors by  $m$  times ( $m$  is to be treated as a parameter). Derive a first order expression for the time it takes for  $V_L$  to settle down within 10% of its final voltage level. Compare the obtained result with the case where no inductance is associated with the wire. Please draw the waveforms of  $V_L$  for both cases, and comment.
- Use the transistors as in part a). Suppose  $C_L$  is changed to 20PF. Sketch waveforms of  $V_S$  and  $V_L$ , assuming a square wave input. Label critical voltages and times.
- Assume now that the transmission line is lossy. Perform Hspice simulation for three cases:  $R=100 \Omega/cm$ ;  $R=2.5 \Omega/cm$ ;  $R=0.5 \Omega/cm$ . Get the waveforms of  $V_S$ ,  $V_L$  and the middle point of the line. Discuss the results.

## 2. Delay line.

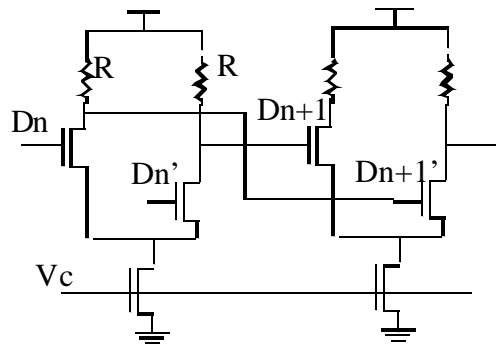


Figure 2: Differential delay element.

Design a delay line composed of the differential delay element pairs from Figure 2.

- Set  $V_{DD}=1.5V$ , and the differential signal swing = 1 V. Please design a delay element pair with 1ns delay, by sizing the transistors, choosing appropriate values for R and  $V_c$ .
- Design an adjustable resistor for the above delay element.
- Derive a first-order expression for the supply sensitivity and run a simulation to verify the result.

## 3. Ling adder

Read the article “A sub-nanosecond  $0.5\mu m$  64 b adder design,” by S. Naffziger presented at 1996 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 362-363.

- Reconstruct the key logic equations in the design of this adder.
- List the four key items that result in speed performance of this adder.