

## HOMEWORK 5.

Due: Friday, April 28, 2000 at 5pm in 558 Cory

**This is an individual assignment!****1. Timing.**

A synchronous mixed-signal chip designed to work at 500MHz has the same clock source, but independent clock trees for A/D converter and digital baseband signal processor.

Both clock tree insertion delays are dependent on operating conditions. ADC clock insertion delay is  $1.5\text{ns} \pm 0.2\text{ns}$ , and the digital clock tree insertion delay is  $2\text{ns} \pm 0.2\text{ns}$ . Additionally, the local skew of both clocks is  $\pm 100\text{ps}$ . The ADC output register and the receiving flip-flop on the digital side are edge-triggered and have setup times of 100ps, clock-to-output delays of 250ps and 100ps hold times.

Derive the minimum and maximum logic delays for the block of combinational logic between the ADC registers and flip-flops on the digital side.

**2. Timing.**

For the L1-L2 latch based system from Figure 2.a. with two overlapping clocks from Figure 2.b. derive all the necessary constraints for proper operation of the logic. The latches have setup times  $T_{SU1}$  and  $T_{SU2}$ , data-to-output delays  $T_{D-Q1}$  and  $T_{D-Q2}$ , clock-to-output delays  $T_{Clk-Q1}$  and  $T_{Clk-Q2}$ , and hold times  $T_{H1}$  and  $T_{H2}$ , respectively. Relevant clock parameters are illustrated in Figure 2.b. The constraints should relate the logic delays, clock period, overlap time,  $T_{ov}$ , pulse widths  $PW1$  and  $PW2$  to latch parameters and skews.

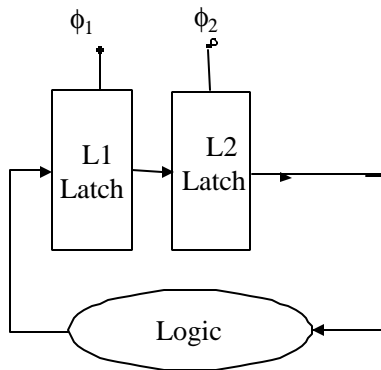


Figure 2.a

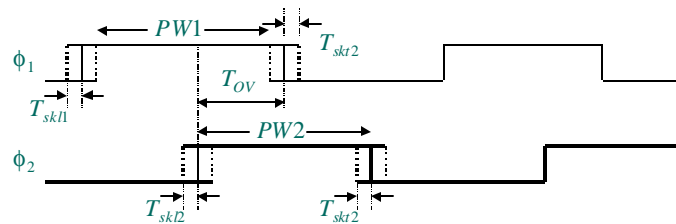


Figure 2.b

**3. Flip-Flop.**

Figure 3. shows a flip-flop that attempts to statistically reduce power dissipation, using a data-transition-lookahead technique.

- Briefly describe the operation of the circuit.
- Is the schematic correct? If not, draw the correct schematic that correctly performs a flip-flop function.
- If all the NMOS transistors are of the same size, and all the PMOS transistors are of the same size, two times wider than NMOS, roughly determine the switching probability of

the input under which this flip-flop reduces power, as compared to an equivalent flip-flop without data transition lookahead circuitry.

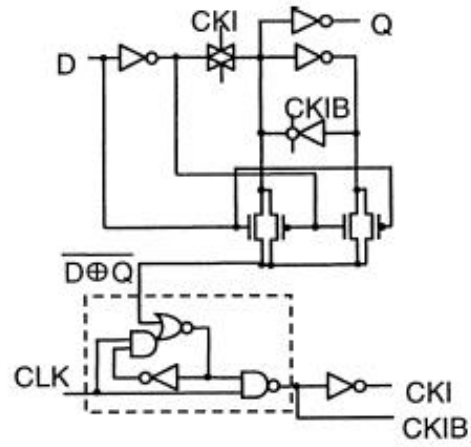


Figure 3.