

Arcadia Parasitic Extraction Flow:

1. Generate schematic netlist and stream out *.gds2 file

- Netlisting:
 - Create symbol view of your circuit.
 - Instantiate it in another cct and Generate netlist (to make it subcct)
- Streaming out *.gds2 file:
 - From “CIW/File” choose “Export/Stream”
 - Specify “Run Directory”, “Library Name”, “Top Cell Name”, check “Stream DB”, and specify “Output File” as “name.gds2”
 - Click on “User Defined Data” and specify “Layer Map Table”, which is: “/tools/unicad/DK_HCMOS7_13_Rev03/hcmos7/hcmos7_13/lyr_filinout_08”
 - Choose “Convert Pin” to “geometry”

2. Generate Calibre Flat Database / Customize Arcadia LVS Rules File

- From “CIW/*Design Kit/Design-Kit Unix interface...”
Select “Layout Design/Arcadia Full Customization/Calibre LVS for Arcadia”
- Template File and Run Directory as well as other settings will be automatically selected, click “OK”
- Fill out layout: gds2 file name, and primary cell name, source spice file name and primary cell name and then click “OK”

3. Produce FLAT calibre database as required by Arcadia

- The following command must be used:
calibre -lvs -bpf -ixf -nxf -nl lvs.ctrl > lvs.log &
- “cd” in the unix directory where caliber LVS has been run
- Type “**bpfToArcadia**”

4. Arcadia Technology File

- From “CIW/*Design Kit/Design-Kit Unix interface...”
Select “Arcadia Full Customization” and then “Arcadia Technology File”

5. Database Translation & Arcadia Extraction

- “cd../RCextArcadiaRunDir”
- Run the ICVERIFYIN command:
ICVERIFYIN ‘tech file’ > icvin.log &
- Run the RCEXTRACT command (make sure you have EMP_CAP_M7.TAB file):
RCEXTRACT ‘tech file’ -f ‘rc_ctrl-file’ -net netfile > rcextract.log &
- Generate SPICE netlist using NETLISTER command:
NETLISTER ‘tech file’ -bn -f ‘netlist_ctrl-file’ -net netfile > netlister.log &
- Translate SPICE netlist to SPECTRE netlist:
“**spice2spectre**” script: “/hitz/users/dejan/calibre/SDRV3300/RcextArcadiaRunDir” does this, but you might need to adjust it if you use different ‘rc_ctrl-file’ and/or ‘netlist_ctrl-file’ commands

Appendix: Control files needed for RC extraction and netlisting:

- netfile: “/hitz/users/dejan/ calibre/SDRV3300/RcextArcadiaRunDir/netfile”

```
*all
~schematic-net-name
vdd! 7 serial-parallel
gnd! 7 serial-parallel
```
- rc_ctrl-file: “/hitz/users/dejan/ calibre/SDRV3300/RcextArcadiaRunDir/rc_ctrl”

```
antenna-diode = no
```
- netlist_ctrl-file : “/hitz/users/dejan/ calibre/SDRV3300/RcextArcadiaRunDir/netlister_ctrl”

```
merge-parallel-mos = yes
feed-through-net = no
calculate-dev-cap = no
conn-substrate = yes
disable-virtual-pins = yes
output-sdpath-xtor = no
preserve-probe-text = yes
show-shortcd-resistor = no
spectre = yes
use-orig-name = yes
reduce = serial-parallel
```
- spice2spectre: “/hitz/users/dejan/ calibre/SDRV3300/RcextArcadiaRunDir/spice2spectre”

```
Type: spice2spectre SPICE.SPI spectre_netlist
```

Note: after running this script you still have to replace vdd_ and gnd_ with vdd! and gnd!, and to delete “-1” before transistor model name in several places

References:

- [1] “/tools/synopsys/epic5.3/documents/Arcadia/User/ArcadiaUser.pdf”
- [2] “/tools/synopsys/epic5.3/documents/Arcadia/Ref/ArcadiaRef.pdf”
- [3] Unicaad documentation: type “unidoc” and select “Design Kit/DK_cmos7 3.0 Manual”