

An Ultra-Low Power Injection Locked Transmitter for Wireless Sensor Networks

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Abstract — This paper presents an ultra-low power, low voltage injection locked transmitter for wireless sensor networks. The transmitter utilizes Film Bulk Acoustic Resonator (FBAR) to obtain a stable 1.9 GHz carrier and achieves 32% efficiency while delivering 0 dBm from a 280 mV supply. With 50% on-off keying, it consumes 1.6 mW and supports a maximum data rate of 50 kbps. The transmitter is implemented in a standard 130nm CMOS process and packaged using chip-on-board techniques.

Index Terms — Transmitter, injection locking, FBAR, MEMS, low power, wireless sensor networks.

I. INTRODUCTION

Recent advances in MEMS technology, coupled with low power, low cost digital and RF circuits have made it conceivable to build a dense network of inexpensive wireless nodes, each having sensing, computational and communication capabilities [1]. These wireless sensor networks are expected to be widely used in a vast variety of applications such as office environmental control, warehouse inventory, smart homes, interactive toys and data collection. One of the key challenges to widespread deployment of such networks is to reduce the node's energy consumption, since it is infeasible to replace batteries of thousands of sensor nodes or attached a large energy scavenging unit to each node. Amongst all its functions, communication between nodes typically accounts for most of the energy budget and hence, it is essential to have an energy efficient transmitter.

The transmitter efficiency η_{TX} can be expressed as:

$$\eta_{TX} = \frac{P_L}{P_{PA} + P_{Pre-PA}} = \frac{1}{\frac{1}{\eta_d} + \frac{P_{Pre-PA}}{P_L}}, \quad (1)$$

where P_L is the radiated power, P_{PA} is the power amplifier's (PA) power dissipation, P_{Pre-PA} is the total power consumption of all the stages prior to the PA and $\eta_d = P_L/P_{PA}$ is the PA's drain efficiency. In wireless sensor networks, each node is spaced less than 10 m apart and the required radiated power is small (~1 mW). At such low radiated power levels, P_{Pre-PA} can represent a large overhead and degrade the transmitter efficiency significantly. For example in [2], the PA achieves a drain efficiency of 40% while delivering 250 μ W but the pre-PA stages consumes 675 μ W, reducing the transmitter efficiency to 19%. Obtaining high

η_d and low P_{Pre-PA} at low radiated power levels is particularly challenging since an efficient PA often requires higher drive voltages or loads its driving stage considerably.

In this paper, we propose using injection locking and RF MEMS to achieve a better compromise between P_{Pre-PA} and η_d at low radiated power levels. Injection locking allows the PA to be self-driven and minimize the loading on its driver, while high-Q RF MEMS allows for ultra-low power RF carrier generation. Using these techniques, the pre-PA power is reduced to 90 μ W and the transmitter achieves 32% efficiency at 0 dBm output power.

II. TRANSMITTER ARCHITECTURE

The block diagram of a conventional transmitter [2-4] and the injection locked transmitter are shown in Fig. 1.

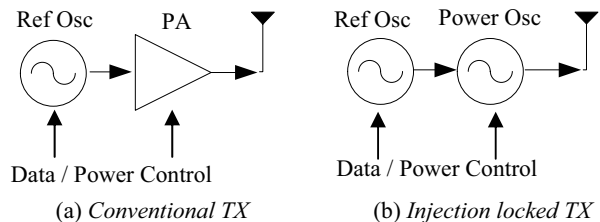


Fig. 1: Low power transmitter architectures.

In the injection locked transmitter, the power amplifier is replaced by an efficient power oscillator. The power oscillator is self-driven and hence does not load the reference oscillator significantly. Due to its low output tank Q, the power oscillator suffers from poor phase noise and has an unstable oscillation frequency. To obtain an accurate carrier frequency, the power oscillator is locked to an ultra-low power reference oscillator, whose oscillation frequency is stabilized by a high Q Film Bulk Acoustic Resonator (FBAR) [5]. Baseband data is modulated onto the carrier by power cycling the power oscillator (on-off keying). Frequency shift keying can be employed using a tunable FBAR oscillator.

III INJECTION LOCKED POWER OSCILLATOR

A. Circuit Design

The schematic of the power oscillator is shown in Fig. 2. The oscillator core consists of cross-coupled transistor pair M_1 - M_2 to provide sufficient negative resistance for oscillation and a LC tank. Three parallel cross-coupled transistor pairs with binary weighted widths (M_3 - M_8) are

used for power control [6]. Parallel devices are preferred over a programmable tail current source because it maximizes the available voltage swing, resulting in higher efficiency. The 50Ω antenna is converted into a 200Ω differential load R_L with a 1:4 balun. This allows the power oscillator to deliver 1mW from a supply of ~ 300 mV.

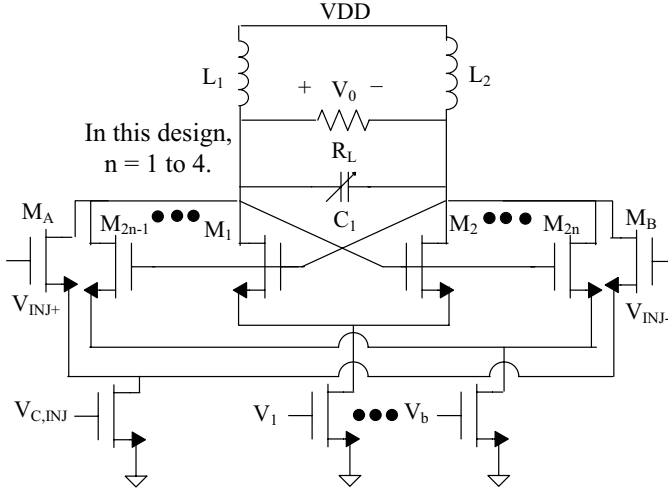


Fig. 2: Schematic of the injection locked oscillator

Transistor M_A and M_B are the injection locking devices used for synchronizing the oscillation frequency ω_0 to the carrier frequency ω_1 provided by the reference oscillator. Since the power oscillator is self driven, the widths of transistors M_A - M_B are chosen to be small to minimize the loading on the reference oscillator and improve reverse isolation. However, this trades off with the lock-in range and lock-in time as discussed in the next sub-section.

A 5-bits switched capacitor array C_1 is employed to mitigate the variations of the bond wire inductance and ensure that ω_0 lies in the lock-in range. The LSB of the capacitor array C_1 is chosen such that $|\omega_0 - \omega_1| \leq 2$ MHz to reduce the lock-in time. The switches are sized such that the Q of the capacitor array is > 60 to minimize losses.

The transistor pairs M_1 - M_8 and M_A - M_B are each controlled by a foot switch to enable on-off keying modulation.

B. Lock-in Range and Lock-in Time

In the absence of the injected signal V_{INJ} , the oscillator oscillates at its free running frequency ω_0 . When the injected signal is applied and if ω_0 lies in the lock-in range, ω_0 will be pulled towards ω_1 . This process is described by the Adler's equation [7,8] given as

$$\frac{d\theta}{dt} = \omega_0 - \omega_1 - \frac{\omega_0 I_{INJ}}{2Q I_T} \sin \theta, \quad (2)$$

where I_{INJ} is the peak current of the injected signal, I_T is the peak fundamental current through the negative resistance, Q is the tank quality factor and θ is the phase difference between V_0 and V_{INJ} . At steady state, $d\theta/dt = 0$ and since

$|\sin \theta| \leq 1$, the single sided lock-in range ω_L is

$$\omega_L = \omega_0 - \omega_1 = \frac{\omega_0 I_{INJ}}{2Q I_T}. \quad (3)$$

The tank Q and I_T is determined by the output power, antenna load and tank inductance. Hence, to widen ω_L , I_{INJ} has to increase, implying a larger loading on the reference oscillator. In this design, $\omega_0 \approx 1.9$ GHz, $Q \approx 4$ and I_{INJ}/I_T is chosen to be 5%, resulting in a lock-in range of ± 12 MHz. This is sufficient since the capacitive array C_1 has a resolution of 4 MHz, ensuring $|\omega_0 - \omega_1| \leq 2$ MHz.

The maximum data rate of the transmitter depends on the lock-in time. The pull-in process is obtained by solving (2), which gives

$$\theta(t) = 2 \tan^{-1} \left[\frac{1}{\sin \alpha} - \cot \alpha \tanh \left(\frac{\omega_L \cos \alpha}{2} (t - t_0) \right) \right], \quad (4)$$

where $\alpha = \sin^{-1}[(\omega_0 - \omega_1)/\omega_L]$ is the steady state phase shift between V_{INJ} and V_0 , and t_0 is the integration constant depending on the initial phase difference θ_i between V_{INJ} and V_0 at $t = 0$. When the injected signal is applied, θ_i will initially approach α at a rate which strongly depends on $(\omega_L \cos \alpha)$. When $\theta(t) \approx \alpha$, this process becomes exponential with time constant ω_L . Hence, for a fast pull-in time, it is desirable to have a large I_{INJ} and a small $(\omega_0 - \omega_1)$. In this design, $|\omega_0 - \omega_1| \leq 2$ MHz, $\omega_L = 12$ MHz, implying $\alpha \leq 10^\circ$ and $\omega_L \cos \alpha \geq 11$ MHz. Using (4), the trajectory of $\theta(t)$ for all possible of θ_i when $\alpha = 10^\circ$ is shown in Fig. 3. For all possible values of θ_i , $\theta(t)$ converges to α in less than 300 ns.

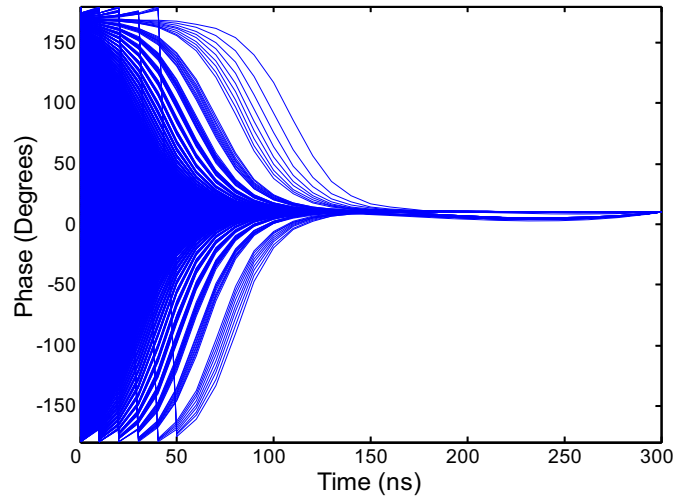


Fig. 3: Trajectory of phase difference between V_{INJ} and V_0 $\theta(t)$ for $0 \leq \theta_i \leq 360^\circ$ with $\alpha = 10^\circ$

IV. ULTRA-LOW POWER FBAR OSCILLATOR

The schematic of the ultra low power reference oscillator [9] is shown in Fig. 4.

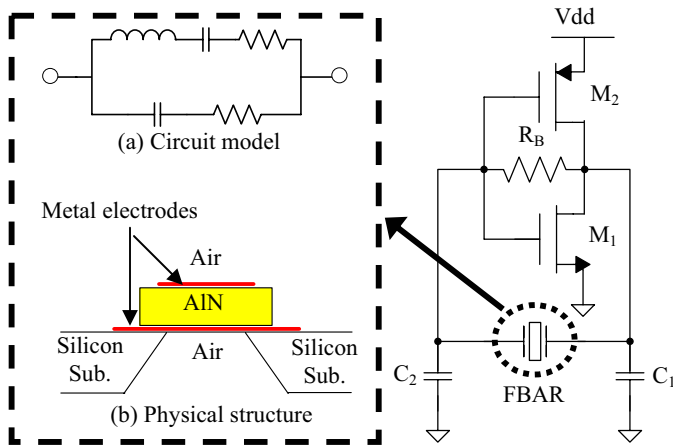


Fig. 4: Schematic of the FBAR oscillator. Inset shows the (a) circuit model and (b) structure of the FBAR.

The reference oscillator employs a high Q FBAR resonator to provide a stable 1.9 GHz carrier while consuming 90 μ W. The FBAR [5] consists of a metal/AiN/metal stack supported by a micro-machined silicon substrate. The metal/air interfaces serve as excellent reflectors to minimize losses. The unloaded Q of the FBAR resonator is > 1000 and it occupies about $100 \mu\text{m} \times 100 \mu\text{m}$. The FBAR is modeled as a RLC circuit as shown in Fig. 4(a).

The FBAR oscillator uses the Pierce configuration with a CMOS inverting amplifier. Transistors M1 and M2 share the same current but their transconductances sum, thus reducing the power consumption by half. A large resistor R_B is used to bias the gate and drain voltage of transistors M1 and M2 at $V_{dd}/2$ to maximize the allowable voltage swing and minimize its loading on the resonator. Detailed analysis and performance of the FBAR oscillator are given in [9].

V. EXPERIMENTAL RESULTS

The power oscillator is implemented in ST Microelectronics $0.13 \mu\text{m}$ CMOS process and packaged using chip-on-board technology. The injected signal is fed from the FBAR oscillator through a balun and oscillator's output is connected to the 50Ω antenna through a 1:4 balun as shown in Fig. 5.

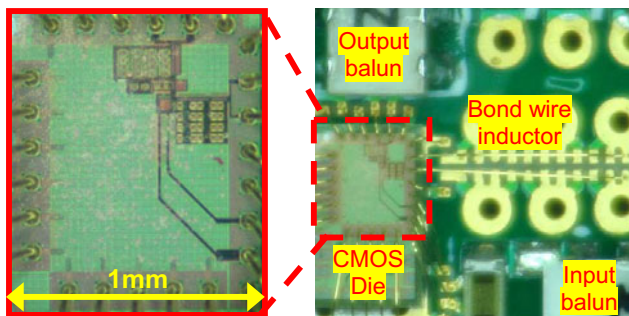


Fig. 5. Close-up of the PCB (right) and die photo (left).

Fig. 6 shows the transmitter efficiency as a function of the radiated power for various supply voltages at $\omega_1 = 1.882$ GHz. Power control of the transmitter is realized using 3 binary weighted cross-coupled transistors (M_3 - M_8). The dotted line shows the maximum achievable efficiency without constraining the supply voltage. At nominal supply of 280 mV, the transmitter achieves an efficiency of 32% while delivering 1 mW. The transmitter can operate with supply voltages as low as 210 mV. At 210 mV supply, it delivers 300 μ W with 25% efficiency.

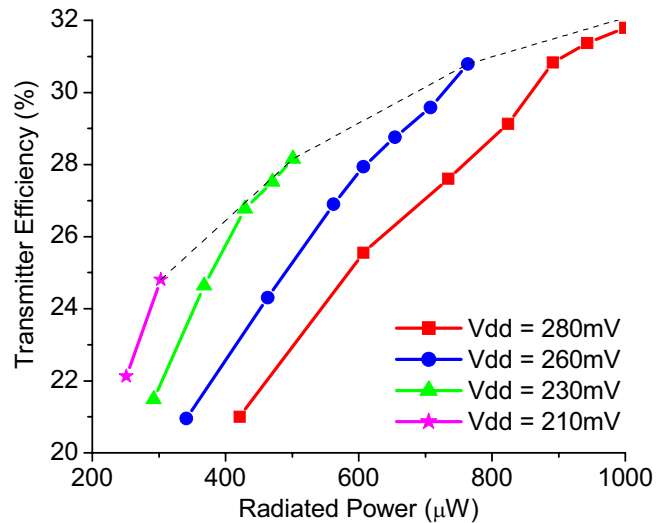
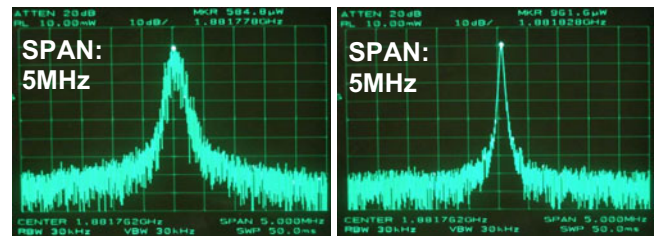


Fig. 6: Measured transmitter efficiency

The output spectrum of the transmitter before and after locking is shown in Fig. 7. Due to the low output tank Q, the output spectrum is broad and noisy prior to locking. When the power oscillator is locked to the FBAR oscillator, it tracks the phase of the reference oscillator and its phase noise performance follows that of the FBAR oscillator. The FBAR oscillator has an excellent phase noise performance of -98 dBc/Hz, -120 dBc/Hz and -138 dBc/Hz at 10kHz, 100kHz and 1MHz offset respectively [9]. This results in a clean and stable carrier frequency as shown in Fig 7(b).



(a) Free running spectrum (b) Locked spectrum

Fig. 7: Transmitter output spectrum

Fig. 8 shows the measured single sided lock-in range ω_L as a function of the bias current of the injection locking transistor M_A . The bias current increases as the lock-in range is increased, degrading the overall efficiency. To reduce the lock-in power, a 5-bit capacitor array is used to tune ω_0 close to ω_1 . As shown in Fig. 9, the capacitive array has a tuning range of 103 MHz with resolution ≤ 4 MHz.

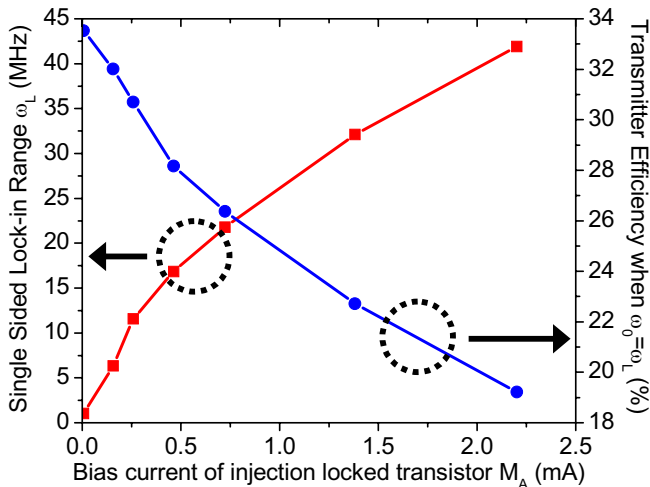


Fig. 8: Measured lock-in range

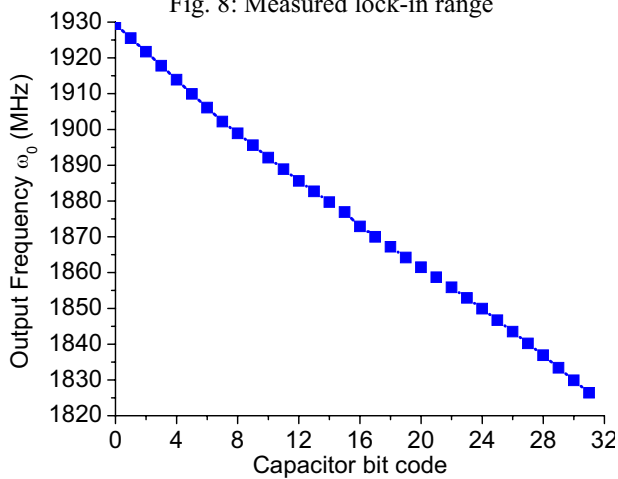


Fig. 9: Measured tuning range of capacitor array C_1

For $\omega_0 - \omega_1 = 2$ MHz, the measured lock-in time is 1.9 μ s. The start up time of the power oscillator is less than 100 ns. Thus the transmitter can support on-off keying modulation with a maximum data rate of 50 kbps if the overhead time is 10% of the symbol period. The modulated on-off keying waveform is shown in Fig. 10.

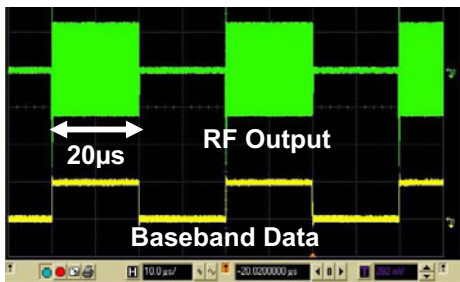


Fig 10: Waveform of on-off keying data.

VII. CONCLUSION

We presented an ultra-low power, low voltage 1.9 GHz injection locked transmitter for wireless sensor networks. It employs RF MEMS and injection locking to achieve better tradeoffs between the PA efficiency and pre-PA power

consumption at low radiated power levels. The transmitter achieves 32% efficiency while delivering 0 dBm from a 280 mV supply. With 50% on-off keying, it consumes 1.6 mW and supports data rate up to 50 kbps. This transmitter compares favorably with other state-of-the-art low power transmitters as shown in Table 1.

Table 1: Comparison with existing low power transmitters

| Ref. | Frequency (GHz) | P_{radiated} (mW) | η_{TX} (%) |
|------------------|-----------------|----------------------------|------------------------|
| This work | 1.9 | 1 | 32 |
| [2] | 0.9 | 0.25 | 19 |
| [3] | 1.9 | 0.5 | 23 |
| [4] | 1.9 | 1.4 | 17 |
| [10] | 2.4 | 1 | 3 |

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