

# A Sub-100 $\mu$ W 1.9-GHz CMOS Oscillator Using FBAR Resonator

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**Abstract** — This paper presents an ultra-low power CMOS oscillator using Film Bulk Acoustic Resonator (FBAR). The 1.9-GHz oscillator consumes 89 $\mu$ W from a low supply voltage of 430mV and achieves an excellent phase-noise performance of -98 dBc/Hz, -120 dBc/Hz and -138 dBc/Hz at 10kHz, 100kHz and 1MHz offset respectively. The oscillator is implemented in a standard 130nm CMOS process and packaged using chip-on-board techniques. Compared with other state-of-the-art oscillators, this oscillator has the best figure-of-merit [1]. To the authors' knowledge, this is the first sub-100 $\mu$ W GHz-range oscillator reported.

**Index Terms** — FBAR, MEMS, low power, oscillators, phase noise.

## I. INTRODUCTION

Gigahertz range oscillators are essential building blocks in today's communication, computing and networking systems. These applications require a small form factor, low cost, low power and low phase noise oscillator. For example, in wireless sensor networks, the average power of the sensor node needs to be 100's of  $\mu$ W to enable energy scavenging while its size has to be  $< 1\text{cm}^3$  [2].

On-chip CMOS LC oscillators are fully integrated but consume more power and have mediocre phase-noise performance [3]. Alternatively, using high Q off-chip resonators (ceramic, SAW and transmission line resonators) leads to lower power dissipation and better phase noise performance but are more bulky [4-6].

Unlike other resonators, FBAR [7] offers both small size and high Q simultaneously. Coupled with good circuit design, this leads to a compact, low power and low phase noise oscillator. In addition, they can be integrated with active devices to form a fully integrated, low cost solution [8].

This paper describes the design and implementation of a 1.9 GHz ultra low power FBAR oscillator with good phase noise performance. The paper is organized as follows: section II presents the characteristics of the FBAR, section III explains the techniques used in low power oscillator design, section IV illustrates its implementation, section V discusses the experimental results and section VI concludes this paper.

## II. FBAR RESONATOR

The FBAR [7] consists of a thin layer of piezoelectric Aluminum-Nitride sandwiched between two metal electrodes, which are supported by a micro-machined substrate as shown in Fig. 1. The metal/air interfaces serve as excellent reflectors to form a high Q acoustic resonator. The unloaded Q of the FBAR resonator is  $>1000$  and it occupies about  $100\mu\text{m} \times 100\mu\text{m}$ .

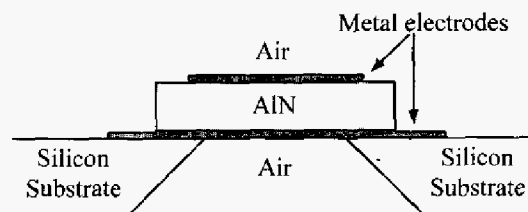


Fig. 1 Cross-section of the FBAR resonator

The FBAR resonator can be modeled using the Modified Butterworth Van Dyke circuit as shown in Fig. 2 [9].  $L_m$ ,  $C_m$  and  $R_m$  are its motional inductance, capacitance and resistance respectively.  $L_s$  and  $C_0$  models the parasitic series inductance and parallel plate capacitance due to the two metal electrodes respectively. Electrode and material losses are accounted by  $R_s$  and  $R_0$  respectively.

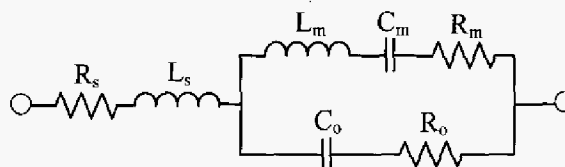


Fig. 2: Circuit model for the FBAR resonator

Fig. 3 shows the frequency response of the FBAR resonator. The FBAR resonator is capacitive at most frequencies except for a narrow band of frequencies between its series and parallel resonance, where it is inductive. In these range of frequencies, the FBAR resonator behaves like a high Q inductor which can be used to build a low power, low phase noise oscillator.

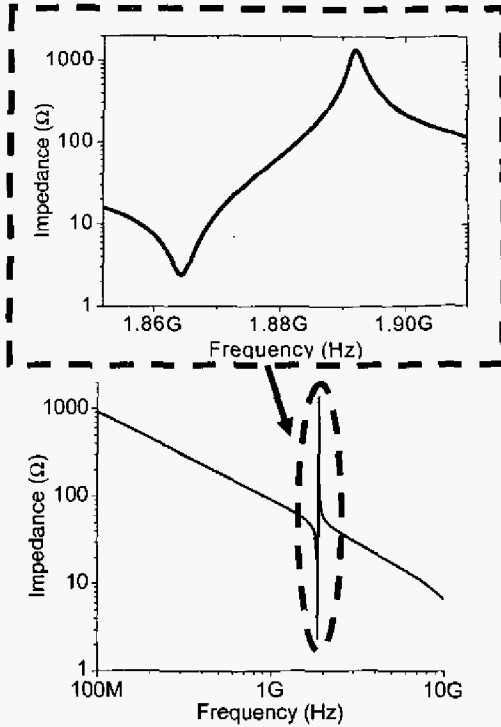


Fig. 3: Frequency response of the FBAR resonator

### III LOW POWER OSCILLATOR DESIGN

The schematic of the oscillator is shown in Fig. 4. The oscillator uses the Pierce configuration with a CMOS inverting amplifier composed of transistor M1 and M2. A large resistor  $R_b$  is used to bias the gate and drain voltage of transistors M1 and M2 at  $V_{dd}/2$  to maximize the allowable voltage swing and minimize its loading on the resonator.

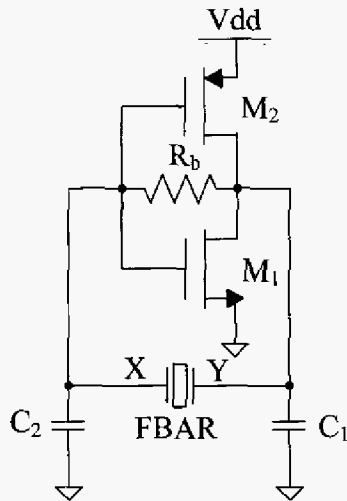


Fig. 4: Schematic of the FBAR oscillator

Transistors M1 and M2 share the same current but their transconductances sum. Thus, only about half the current is needed to provide the necessary transconductance for oscillation. To reduce the power further, the transistors M1 and M2 are designed to operate in the sub-threshold regime to maximize their current efficiency ( $g_m/I_d$ ). In addition, the drain-source voltage of transistors M1 and M2 is designed to be at least a few  $kT/q$  to achieve a high output resistance and minimize its loading on the resonator.

Capacitors  $C_1$  and  $C_2$  transform the transconductance of the inverting amplifier into a frequency dependent negative resistance,  $-R$ . The impedance looking from FBAR (across node X and node Y) is the given as

$$Z = -\frac{G_{m1} + G_{m2}}{\omega^2 C_1 C_2} + \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} \quad (1)$$

where  $\omega$  is the angular frequency and  $G_{m1}$ ,  $G_{m2}$  are the large signal transconductances of transistor M1 and M2.

At the frequency of oscillation  $\omega_{osc}$ , the FBAR behaves like an inductor  $L_{eq}$  in series with resistance  $R_{eq}$ . To sustain steady state oscillation,  $R_{eq} = R$ , or

$$G_{m1} + G_{m2} = \omega_{osc}^2 C_1 C_2 R_{eq} \quad (2)$$

From eqn. (2), small values of  $C_1$  and  $C_2$  are desirable as they require less  $G_m$  to sustain steady state oscillation, resulting in lower power consumption. Thus, for this design, capacitors  $C_1$  and  $C_2$  are solely composed of the transistors' gate and drain capacitances, interconnect capacitances and pad capacitances and no explicit capacitance is added. Also,  $C_1$  is set to be equal to  $C_2$  to yield the best negative resistance at the frequency of oscillation.

### IV. IMPLEMENTATION

The oscillator is implemented in a standard  $0.13\mu\text{m}$  CMOS process from ST Microelectronics. The FBAR resonator and the CMOS die are packaged together onto a test board using chip-on-board techniques as shown in Fig. 5. Two short bond wires are used to connect the FBAR to the CMOS die to minimize parasitic and avoid any spurious oscillations. Each bond wire is estimated to be  $\sim 250\text{pH}$  and is taken into account in the design. The oscillator is connected to an on-chip buffer to provide a  $50\Omega$  output. The entire oscillator is about  $1.7\text{mm} \times 0.8\text{mm}$ . The oscillator core occupies only  $40\mu\text{m} \times 40\mu\text{m}$ . For more compact implementation, the FBAR die can be flip-chip on top of the CMOS die, or the resonator can be integrated with the active devices [8].

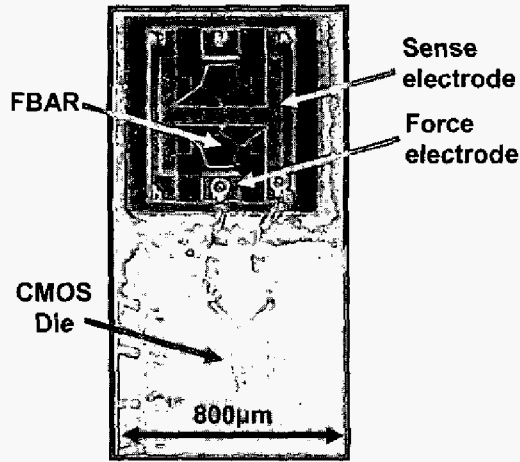


Fig. 5: Die Photo of the FBAR oscillator

As shown in Fig. 5, the bond pads for the FBAR's electrodes are not identical. The smaller force electrode has a pad capacitance of 20fF whereas the larger sense electrode has a pad capacitance of 150fF. On the other hand, the total gate capacitance of M1 and M2 is about 330fF and their total drain capacitance is about 200fF. Thus, connecting the gate node to force electrode and the drain node to the sense electrode results in  $C_1 = C_2$ , which maximizes the negative resistance at the oscillation frequency.

#### V. EXPERIMENTAL RESULTS

The oscillator is self-biased with a 430mV supply and dissipates 89µW for sustained oscillations at 1.882 GHz. The measured zero to peak output swing of the oscillator is 142mV. The output spectrum of the oscillator is shown in Fig. 6. A clean output signal is obtained and no close-in spurs are observed, indicating the absence of low frequency parasitic mechanical resonances. Second, third and fourth and fifth harmonics are measured to be -43.8 dBc, -45.5 dBc, -68.8 dBc and -69.7 dBc respectively.

The phase noise performance is shown in Fig. 7. The measured phase noise at 10kHz, 100kHz and 1MHz offset is -98 dBc/Hz, -120 dBc/Hz and -138 dBc/Hz respectively. Good phase noise performance is mainly attributed to the high Q factor of the resonator.

A better phase noise performance can be obtained by operating the oscillator at the edge of the current limited regime with higher power consumption [1]. Fig. 8 shows the zero-to-peak output voltage swing and measured phase noise for various power consumptions. The best phase noise performance occurs when the output voltage swing is 167mV and oscillator dissipates 104µW. The optimal phase noise is -100 dBc/Hz, -122 dBc/Hz and -140

dBc/Hz at 10kHz, 100kHz and 1MHz offset respectively. Beyond this operating point, the oscillator transits into the voltage limited regime where the output resistance of the transistors decreases and loads the oscillator, resulting in poorer phase noise performance.

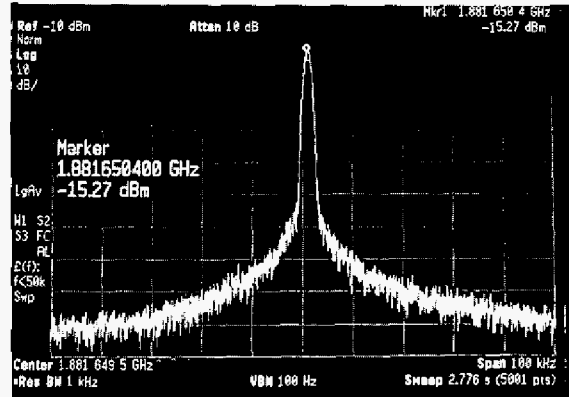


Fig. 6: Output frequency spectrum

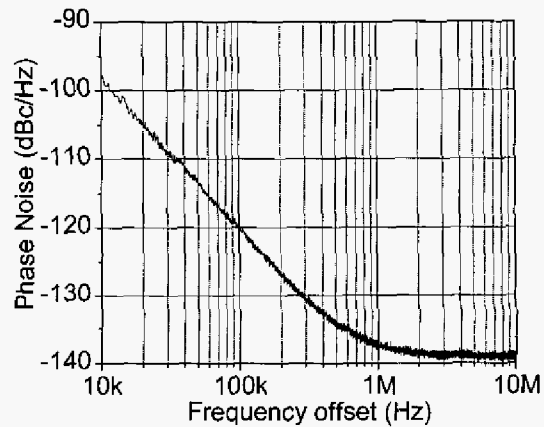


Fig. 7: Measured phase noise performance

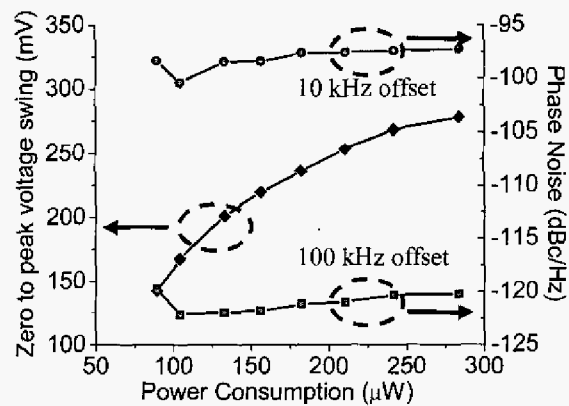


Fig. 8: Measured output voltage swing and phase noise performance for various power consumptions.

Ref.	$f_{osc}$ (GHz)	$P_{DC}$ (mW)	Phase Noise	Process ( $\mu\text{m}$ )	Resonator / Inductor	FOM
This work	1.9	0.104	-122 dBc/Hz @ 100kHz offset	0.13 CMOS	FBAR	43.64
	1.9	0.089	-120 dBc/Hz @ 100kHz offset	0.13 CMOS	FBAR	41.88
[10]	1.9	0.3	-120dBc/Hz @ 100kHz offset	0.18 CMOS	FBAR	37.05
[4]	5.8	40	-106dBc/Hz @ 10kHz offset	0.8 SiGe BiCMOS	SAW resonator	31.11
[5]	5.8	0.328	-115dBc/Hz @ 1MHz offset	0.09 CMOS	Thin film inductor	21.28
[6]	2.4	39	-121dBc/Hz @ 100kHz offset	Si Bipolar	LTCC ceramic resonator	18.75
[3]	5.9	7.65	-124dBc/Hz @ 1MHz offset	0.18 CMOS	On-chip LC	16.89

Table 1: Comparison with state-of-the-art oscillators

To evaluate the performance of this oscillator, a unitless power-frequency-normalized figure of merit (FOM) is used [1]. The FOM is defined as:

$$\text{FOM} = 10 \log \left[ \frac{kT}{P_{DC}} \left( \frac{f_{OSC}}{f_{OFFSET}} \right)^2 \right] - L\{f_{OFFSET}\} \quad (3)$$

where  $P_{DC}$  is the DC power consumption of the oscillator,  $L\{f_{OFFSET}\}$  is the phase noise of the oscillator at an offset frequency  $f_{OFFSET}$  from its oscillation frequency  $f_{OSC}$ ,  $k$  is the Boltzmann constant and  $T$  is the temperature in Kelvin. Table 1 shows that our oscillator has the best FOM compared to other state-of-the-art GHz-range oscillators. In this design, we have used 0.18 $\mu\text{m}$  channel length and hence the 6.6dB improvement over previous design [10] is mainly due to low power circuit design techniques discussed in section III.

## VI. CONCLUSION

We have presented an ultra-low power 1.9-GHz CMOS oscillator using FBAR resonator. The oscillator draws 89 $\mu\text{W}$  from a 430mV supply and achieves a phase-noise of -98 dBc/Hz, -120 dBc/Hz and -138 dBc/Hz at 10kHz, 100kHz and 1MHz offset respectively. Compared with other state-of-the-art oscillators, our oscillator has the best FOM. To the authors' knowledge, this is the first sub-100 $\mu\text{W}$  GHz-range oscillator reported.

This low power oscillator can be employed in a direct modulation transmitter (e.g. for low data rate wireless sensor network applications) where the digital data is modulated on to the RF carrier by on-off cycling the oscillator. Alternatively, a digitally controlled capacitive bank or a varactor can be added for frequency tuning, converting it into a VCO.

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