Yield Optimization with Energy-Delay Constraints in Low-Power Digital Circuits

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***Abstract* – As circuit parametric variations aggravate in advanced technology, yield emerges as an important figure-of-merit in circuit design. Based on a 130nm technology, the yield-energy-delay tradeoffs in low-power circuit optimization are investigated. Using a log-normal statistical model, Monte-Carlo analyses are performed on typical circuit examples, including an inverter chain, NAND gate, and 4-bit adder. While energy reduction can be effectively achieved by tuning supply voltage (V_{dd}), threshold voltage (V_{th}), and device width (W), circuit yield degrades during this process. On the other hand, it is observed that performance variability is relatively insensitive to circuit topology and device length (L). Design guidelines for optimizing yield in the presence of parametric variations and energy-delay constraints are proposed.**

I. INTRODUCTION

The rapid scaling of silicon technology has enabled dramatic success in integrated circuits (ICs) design. Meanwhile, precise control of chip manufacturing becomes increasingly difficult and expensive in the nanometer regime. Silicon processes such as lithography, oxidation, and ion implantation suffer more severe variations as technology scaling continues [1]; in addition, run-time environmental fluctuations (e.g., L(di/dt) noise in V_{dd} and temperature change) also increase as chip operation frequency and power consumption escalate. As a result, circuit performance exhibits much wider variability, leading to increasing yield degradation in successive technology generations. Therefore, the robustness of circuits has emerged as a roadblock in modern IC design [1].

Conventional variation-tolerant design strategies generally rely on optimization of the design at nominal conditions while reserving adequate margins at design corners. However, as performance variability is exacerbated, these margins widen to the extent that this methodology becomes impractical. Furthermore, from experiments and simulations, it is observed that performance variations are not only sensitive to circuit parametric fluctuations (e.g., within-die and die-to-die process variations), but also to nominal values of circuit operation conditions, such as V_{dd} and V_{th} [2]. For instance, while tuning of V_{dd} and V_{th} is an effective technique for energy minimization, this optimization leads to a degradation of circuit yield [2]. Therefore, circuit optimization must be expanded to account for yield concerns with energy-delay specifications.

This work pursues a comprehensive understanding of the impact of various optimization techniques on circuit yield in low-power design. It is organized as follows. The yield definition and circuit performance models are introduced in Section 2. Section 3 presents the experimentation framework and Monte-Carlo analysis on yield-energy-delay tradeoffs for a canonical inverter chain as well as for a NAND chain and 4-bit adder implemented in various logic topologies. In Section 4, design guidelines for maximizing yield with energy-delay constraints are discussed. Section 5 concludes the paper.

II. CIRCUIT PERFORMANCE MODELS

2.1. Yield Definition

Circuit yield refers to the percentage of total circuits whose propagation delays fall within a critical delay cutoff. In the presence of parametric variations, circuit speed is distributed over a range, leading to yield degradation. The performance distribution can be evaluated by the normalized variability, which is $3\sigma/\mu$ (Fig. 1). A larger value of $3\sigma/\mu$ represents a wider distribution and thus a lower yield. To be consistent with this consideration, we define yield at the point where delay is 10% larger than the mean. That is,

$$\text{Cutoff Delay} = (1+10\%) \cdot \text{Delay Mean} \qquad (1)$$

Fig. 1 illustrates such a definition. Furthermore, the correlation between cutoff point and mean reflects the change of design expectation during optimization. In low-power design, circuit speed is usually sacrificed to save power consumption; thus, it is reasonable to scale the cutoff point along with mean to determine yield, instead of using a fixed limit. Note that the choice of 10% is relatively arbitrary as it generates about 95% yield at nominal operation condition.

2.2. Nominal Performance Model

The nominal circuit delay is modeled by the alpha-power law [3]. For a multiple stage circuit, if we assume perfect correlation among stages, which represents the worst case of variability, it can be expressed as:

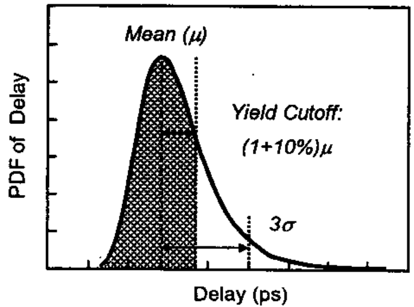

Figure 1. Performance based yield definition.

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$$t_d = \frac{LV_{dd}}{(V_{dd}-V_{th})^{\alpha}}\sum_i\left[\frac{C_{load}}{KW}\left(g+\frac{p}{h}\right)\right]_i \tag{2}$$

Here, α is a fitting parameter whose value depends on the specific process; g, p, and h are logical effort, parasitic delay and electrical effort of the gate. Switching energy is described as:

$$E_a = \sum_i \left(CV_{dd}^{\,2}\right)_i \tag{3}$$

Note that leakage energy is not included in this study since active energy still accounts for the majority of total power consumption. Eqns. (2) and (3) serve as the physical foundations to explain circuit behavior and provide guidelines to yield optimization, which will be discussed in more details in Sections 3 and 4.

2.3. Lognormal Statistical Model

In the analysis of statistical circuit behavior, performance is usually modeled as a normal distribution [2]. However, at low supply voltages (or low V_{dd}/V_{th}), the shape of the circuit performance distribution deviates from a Gaussian shape, due to a nonlinear dependence on process and voltage parameters, as indicated in Eqn. (2). Fig. 2 illustrates the delay distribution of an inverter chain implemented in 130nm technology. The probability density function (PDF) of 5000 Monte-Carlo simulation points has an asymmetrical shape, skewed toward the lower end of the data range. In order to account for this asymmetry, the lognormal model has been used to describe the data. Fig. 2 illustrates that this model fits quite well, with less than 4% cumulative density function (CDF) discrepancy.

The main difference between the lognormal model and normal model lies in their respective mean value predictions. Fig. 3 illustrates this distinction by comparing the mean value of the inverter chain delay as predicted by both models with the mean value generated from nominal design specifications. A valid statistical model should match the nominal result with its mean value; in Fig. 3, it is shown that for various V_{dd} and V_{th}, the lognormal model matches the nominal inverter chain delay. In contrast, for the normal distribution, the matching error under low V_{dd} is nearly 60%. This difference is reduced for high supply voltages. Therefore, we conclude that the lognormal model should be used for statistical analysis, especially in low-power design where supply voltage is usually very low to achieve power reduction.

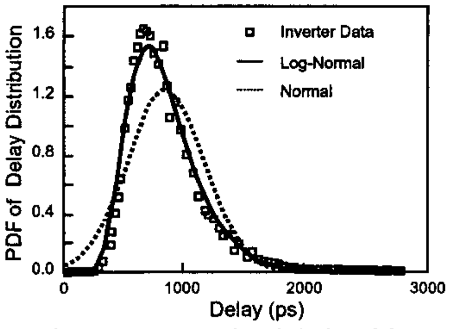

Figure 2. Log-normal statistical model. (V_{dd}=400mV, V_{th}=130mV)

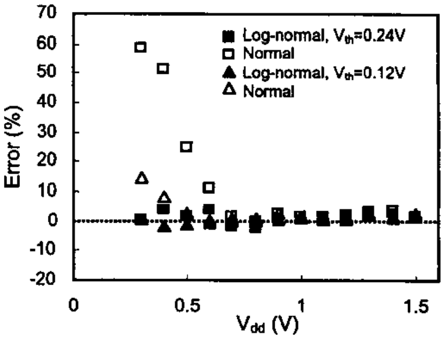

Figure 3. Discrepancy between the nominal delay and model predicted mean values.

III. SIMULATIONS AND RESULTS

3.1. Technology Specifications and Simulation Setup

Since the delay variability is most sensitive to fluctuations in L, V_{dd}, and V_{th}, these parameters are the focus of this study [4]. Other parameters either only have a weak impact on performance in current technology (e.g., parasitic source-drain resistance) or benefit from excellent variation control (e.g., gate oxide). Therefore, their impact is not considered in this work. L, V_{dd}, and V_{th} are modeled as normally distributed random variables. For L, we assume the absolute variation (3σ) remains constant during sizing, which is a pessimistic projection of lithography control. Since the stability of V_{dd} is usually controlled by process-independent design techniques (e.g., adding decoupling capacitance to supply rails), the 3σ/μ of V_{dd} is assumed to be fixed at 10%. In the nanometer regime, V_{th} variation is dominated by channel doping fluctuation and thus relies on device size [5]:

$$\sigma_{V_{th}} \propto \left(W\cdot L_{eff}\right)^{-1/2} \tag{4}$$

Moreover, as a conservative estimate, constant 3σ/μ is assigned to V_{th} in nominal V_{th} tuning. Perfect parameter correlation over stages is assumed in the canonical circuits because of their relatively small size. The detailed technology specifications for variation sources are summarized in Table 1 [4, 6]. These values are applied to canonical test circuits and yield-energy-delay information is extracted from Monte-Carlo SPICE simulations.

3.2. Yield-Energy-Delay Tradeoffs

The main test circuit studied in this section is a five-stage delay-optimized inverter chain driving a 1pF capacitor load, as shown in Fig. 4. Other test circuits include a NAND chain and a 4-bit adder implemented in static CMOS, pass-gate (PTL), and dynamic logic.

TABLE I. TECHNOLOGY SPECIFICATIONS

	Mean	3σ/mean
L_{eff_nmos} (nm)	71	15%
L_{eff_pmos} (nm)	80	15%
V_{th0_nmos} (V)*	0.24	15%
V_{th0_pmos} (V)*	-0.34	15%
V_{dd} (V)	1.2	10%

* This is for minimal sized inverter: W_n=0.585μm.

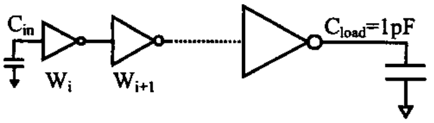

Figure 4. A delay-optimal inverter chain. (W_{1n}=0.585μm, W_{i+1}/W_i=3.6, N=5)

A. V_{dd} and V_{th} Optimization

Tuning V_{dd} and V_{th} has been shown to be one of the most effective techniques for balancing the reduction of active power consumption with sacrifices in performance and leakage. Using the yield definition from Section 2, Fig. 5 shows the dependence of delay, normalized delay variation (3σ/μ), switching energy and yield of the inverter chain on V_{dd} and V_{th}, as derived from Monte-Carlo simulation results. While these results confirm the known trend of delay and energy scaling, it is also observed that the delay variability changes at a similar rate to the nominal delay with V_{dd} and V_{th} tuning. As a result, circuit yield degrades when V_{dd} is lowered or V_{th} is increased. This behavior can be attributed to the non-linear dependence of circuit delay on V_{dd} and V_{th}. According to Eqn. (2), the sensitivity of delay on parameter variations increases with decreasing V_{dd} or V_{dd}/V_{th}, leading to wider variability [2]. Therefore, in order to improve circuit yield, it is desirable to use higher V_{dd} and lower V_{th}, if energy and delay do not exceed specifications.

Furthermore, the result shows that, in contrast to the sharp reduction of switching energy with lower V_{dd}, yield degrades at a much slower rate. For example, when the V_{dd} is reduced from 1.2V to 0.4V (at V_{th}=0.241V), yield degrades from 90% to 60%, while energy is saved by 80%. This relationship indicates that the energy-yield tradeoff is favorable for low power design.

B. Device Width (W) Tuning Effect

Besides V_{dd}/V_{th} tuning, device sizing is another effective technique to optimize energy consumption under delay constraint [3]. In the case of a delay-optimized inverter chain, the switching power consumption can be effectively reduced with a comparatively small delay penalty by systematically shrinking the tapering factor along the path. Here, we use the same sizing rule as in [7]:

$$W_{i+1}/W_i = W_i/W_{i-1} + u\cdot W_i \qquad (5)$$

where W_i is the device width at stage *i*, and *u* is a sizing factor. When u=0, Eqn. (4) gives the delay-optimal condition where the sizes of all stages are uniformly scaled (Fig. 4). Energy is reduced when *u*>0 is applied and inverter size is decreased. Due to the dependence of V_{th} variation on W (Eqn. 4), a device with smaller W suffers larger V_{th} fluctuations and thus a worse yield. The impact of W on yield and energy is illustrated in Fig. 6: when *u* increases from 0 to 0.2, the size of the last inverter in the chain is 14 times smaller and the switching energy is saved by more than 90%; meanwhile, yield may degrade by more than 5%, depending on operation conditions. This phenomenon is particularly severe when V_{dd} is low since circuit variation is svery sensitive to V_{th} in this situation (Fig. 6). Furthermore, ignoring the correlation between W and $\sigma_{V_{th}}$ leads to significant underestimations of yield, as shown in Fig. 6. Due to the yield concern, it is preferred to use large values of W in low power design.

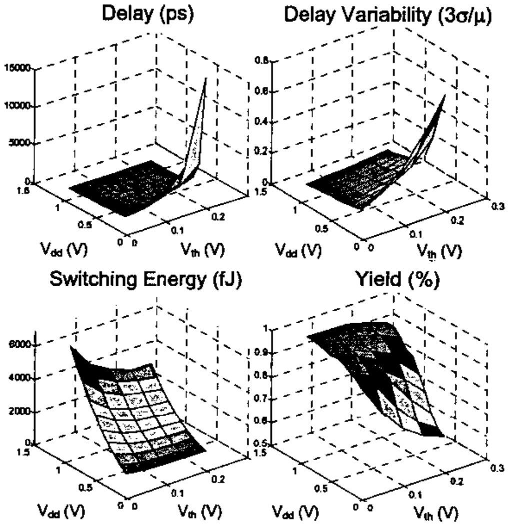

Figure 5. Yield-energy-delay tradeoffs in V_{dd} and V_{th} tuning. (Test circuit: inverter chain)

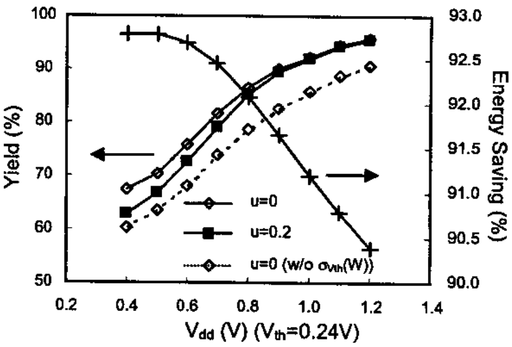

Figure 6. Impact of device sizing on yield.

C. Other Circuit Design Factors

By plotting the yields of the inverter chain, NAND chain, and 4-bit adders of each circuit topology against V_{dd} at fixed V_{th} (Fig. 7), it is observed that the yield of digital logic circuits is relatively insensitive to the type of circuit (inverter or adder) and circuit topology (static CMOS or PTL). This can be explained by Eqn. (2): since electrical and logic efforts, which characterize different logic circuits, do not contribute to delay distribution, their influences are eliminated in normalized performance vari-

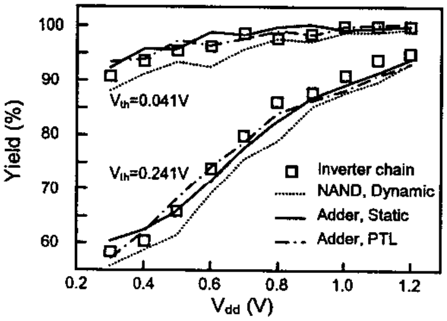

Figure 7. Dependence of yield on circuit topologies.

ability. Therefore, yield is immune to these factors. Note that this conclusion relies on the assumption of perfect correlation over stages; in the case of non-ideal correlation (e.g., strong within-die random variation), yield also depends on the complexity of circuits.

For L tuning, using longer device length suppresses leakage, but causes a heavy penalty in delay and switching energy; moreover, it has only a weak effect on yield. Consequently, in future yield-aware designs, we only need to consider the influences of V_{dd}, V_{th}, and W.

IV. YIELD OPTIMIZATION GUIDELINES

Since yield strongly depends on the nominal circuit operation conditions (V_{dd}, V_{th}, and W), it is necessary to consider yield with the equal importance as energy and delay during circuit optimization. Section 3 demonstrates that yield can be significantly improved by increasing V_{dd}, V_{dd}/V_{th}, or W, as shown in Figs. 5 and 6. Based on these observations, we further investigate the effectiveness of these techniques. Fig. 8 illustrates the sensitivity of yield to the individual tuning of V_{dd}, V_{dd}/V_{th}, and W in an inverter chain (Fig. 4). It is revealed that tuning the ratio of V_{dd} and V_{th} has the largest impact on circuit yield: increasing V_{dd}/V_{th} by 50% can enhance yield from 85% to 95%. On the other hand, the effects of tuning V_{dd} and W are comparable to each other, but have a smaller contribution to yield improvement.

In general, the problem of yield optimization can be refined as the choice of optimal values of V_{dd}, V_{th}, and W, such that delay variation is minimized while nominal energy and delay specifications are satisfied. Considering the delay and switching energy of a single path circuit are governed by Eqns. (2) and (3), respectively, such an optimization can be proceeded as the following: first, increase V_{dd}/V_{th} to a reasonable value, since yield is the most sensitive to V_{dd}/V_{th}; then, scale down V_{dd} to compensate the change in nominal delay; finally, size up W to achieve the same energy consumption, since switching energy is proportional to W. Although increasing W and reducing V_{dd} have opposing effects on yield, overall this process is favorable to yield improvement, as demonstrated in Fig. 9. Fig. 9 shows that for an inverter chain, with W increasing by 75%, V_{dd} reduced from 1.2V to 0.73V, and V_{th} reduced from 0.241V to 0.073V, yield increases from 94.82% to 98.70%, while delay and energy are the same, as summarized in Table 2. For more complicated circuits with multiple data-paths, these guidelines are still applicable to each path.

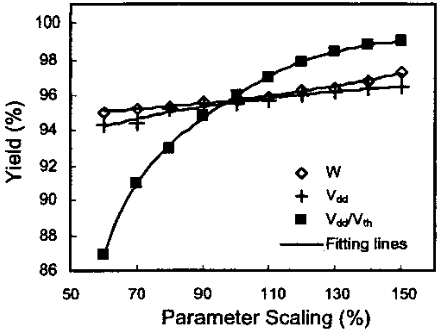

Figure 8. Yield sensitivity to parameter tuning.

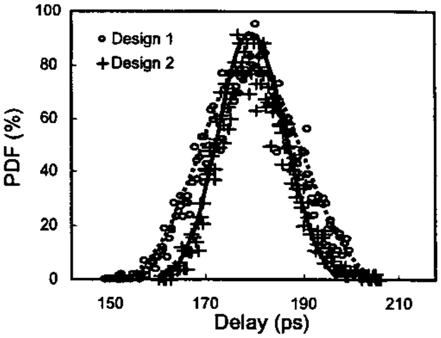

Figure 9. Yield optimization with energy-delay constraints. (Delay=179ps; Energy=757fJ)

TABLE II. DESIGN COMPARISONS

	Design 1	Design 2
W	100%	175%
V_{dd} (V)	1.2	0.73
V_{dd}/V_{th}	4.98	9.96
Yield	94.82%	98.70%

V. CONCLUSIONS

Throughout the study, it is observed that circuit yield degrades with energy reduction. Since this phenomenon is more pronounced under low V_{dd} conditions, it is necessary to consider yield in conjunction with delay and energy concerns in robust low-power circuit optimization. Using Monte-Carlo analysis on a variety of typical digital circuits, we conclude that yield can be maximized by increasing V_{dd}, V_{dd}/V_{th}, and W. By properly scaling up V_{dd}/V_{th} and W, while decreasing V_{dd}, optimal yield can be achieved under the same constraints of delay and energy. Based on these results, we expect to develop more efficient yield-aware optimization methodology for future robust low-power circuit design.

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