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## ABSTRACT

Based on the modified nodal analysis of switched capacitor (S.C.) networks very efficient time, frequency, sensitivity and noise simulation of S.C. networks, A/D, D/A converters and digital filters is possible. Primitives range from high level (op-amps, registers) down to transistor level. This makes it possible to use the same program DIANA from concept verification down to transistor circuit design. Circuits can be linear or non-linear, continuous or/and sampled and frequency analysis includes aliasing and folding effects.

## INTRODUCTION

Sampled data MOSLSI circuits are used intensively in VLSI circuitry for telecommunication and control systems. They include switched capacitor filters, A/D and D/A converters, analog multiplexers as well as digital filter structures. Common characteristics to such circuits are :

1. mixture of analog and digital circuits
2. time variant character
3. large ratio between sample- $(f_s)$  and signal frequency  $(f)$ .

Characteristic 1. suggests the use of a mixed-mode (hybrid [1]) simulation program i.e. the combination of circuit-timing- and logic (functional) simulation in one program using a common input language.

However, such programs do not allow for efficient simulation of sampled analog and/or digital networks, due to characteristics 2. and 3. and the lack of frequency, sensitivity and noise analysis. In this paper it will be shown how new theoretical work [2] [3] [4] on S.C. networks can be implemented in the existing mixed-mode simulator DIANA. This makes it possible to get efficient time, frequency, sensitivity and noise analysis of S.C. and digital circuits. In this way DIANA becomes a single design tool for sampled-data circuits from concept down to transistor and gate level.

## THE DIANA PROGRAM : TIME DOMAIN SIMULATION

As shown in Fig. 1 DIANA has four modes of simulation (I-IV) of which circuit, timing and logic (II-IV) can be mixed in the same run. In this way circuits up to 5000 gate complexity have been simulated from register down to transistor level. New is the sampled-data mode I. In this mode the primitives are resistorless elements including ideal clocked (capacitive) switches, analog multipliers, adder-subtractors and periodically clocked delay blocks. The latter three primitives are of interest to digital filter structure simulations. Mode I is a conceptual level in which sampled-data network behavior is considered as a succession of equilibrium states after each clock  $(\phi(t))$  transition. The validity of this assumption can be checked at a lower level (e.g. mode II).

The authors have shown elsewhere [2] [3] [4] that such networks can easily be described in the Modified Nodal Analysis (MNA) matrix formalism which is used in most CAD programs.

The technique is based on charge conservation during switching and coincides with Backward Euler integration with unity time step. It is therefore directly compatible with the CAD formalism used in DIANA for mode II simulation. No approximations are involved.

In this way, voltages (V) and charges (Q) can be computed from one time slot to the next. This greatly speeds up the simulation with respect to classical transient analysis which requires too many time points/time slot to obtain reasonable accuracy.

The advantages of this technique are :

- arbitrary clock sequences possible;
- all switch configurations allowed;
- with Newton-Raphson per time slot also nonlinear effects are simulated;
- after verification at conceptual level, modes II, III and IV can be used for more detailed simulation (second order effects) when design is refined.

## EXAMPLE OF TIME DOMAIN SIMULATION

Fig. 2a represents a simple pole-zero stage using an op-amp (XVA) with gain  $10^3$ . Also shown is the input to DIANA for this circuit in mode I. Notice that use is made of capacitive double throw switches driven by clock CLX. Time step unit is  $5 \mu s$ . Fig. 2b shows the simulated unit-sample time response to a voltage input during time slot  $Cl_2$  ( $5-10 \mu s$ ).

Such a unit sample response is the basis for frequency analysis as will be discussed in next paragraph. This mode I simulation can be used to study amongst others :

- DC drift due to op-amp offset;
- DC drift due to non-linear junction; capacitors
- Distortion of sinusoidal inputs;
- Study of capacitor errors and offset in A/D converters;
- Impulse response of digital filters etc...

When the network concept has been checked one can, using the same hierarchical input language, go to other simulation modes or mixtures thereof to study second order effects such as detailed time response, clock feedthrough, strong effects, digital-analog circuitry interactions, op-amp design, digital filter logic design etc...

As an example, Fig. 3a shows the same filter as in Fig. 2a but now described with PASS transistor models (Fig. 1), including nonlinear capacitor effects and a one-pole op-amp model (mode II). The feedback capacitors are controlled by a digital circuit described in mode IV (logic simulation). Fig. 3b is an output plot of a true mixed-mode

simulation of this letter for a 10 kHz sinusoidal input ( $V_{in}$ ) under digital control (FFC, UP, DOWN).  $V_{in}$  is the op-amp input and  $V_{out}$  the output voltage. The plot shows clearly clockfeedthrough effects and even a spike. A resulting from a hazard in the digital control circuit.

In this example 1800 time points of  $1\mu s$  have been simulated in 120sec. CPU on IBM 370/158.

Fig. 4 is the simulation of a 8 bit A/D converter including successive approximation logic (Modes II & IV). Shown are the comparator input, clock and register output. Transient analysis for 600 points takes 8.3 sec CPU on IBM 3033.

#### FREQUENCY DOMAIN-SENSITIVITY & NOISE ANALYSIS

For a sampled data system with one single unit sample response the frequency response can be obtained directly from a Fast Fourier Transform of this response. However S.C. networks are time-variant with a multiphase T-periodic clock, potentially with a direct capacitive input-output (I/O) coupling and continuous input. The output can be sampled (and held) during a single or more time slots/clockperiod and aliasing effects need to be considered.

For example the circuit in Fig. 2a has two different unit sample responses (time slots  $C1_1, C1_2$ ) to be considered during two different time slots at the output i.e. four unit sample responses  $h_{i,j}(n)$ ;  $i, j = 1, 2$  exist. Moreover the path through  $C_1, C_0$  is a continuous I/O path.

In [2] [3] and [4] the authors have shown that :

- a) For all possible cases, including continuous I/O path, continuous input & multiphase output, the frequency response can be computed from the FFT's  $H_{i,j}(e^{j\omega T})$  of all unit sample responses  $h_{i,j}(n)$  which can be computed in mode I. If there are  $N$  time slots per period,  $N$  analyses may be necessary but :
- b) For every S.C. network  $\mathcal{N}$  an adjoint S.C. network  $\mathcal{N}^*$  exists of which the MNA is the transposed of that of  $\mathcal{N}$ . For a clock with  $N$  time slots and one output sample per clock period the following holds :
  - b-1) The frequency response of  $\mathcal{N}$  can be obtained from only one unit sample analysis of  $\mathcal{N}^*$ ;
  - b-2) The sensitivity of amplitude and phase with respect to all network parameters and frequency can be obtained from  $N$  nominal and one adjoint network analyses;
  - b-3) When  $n$  noise sources are present the noise spectrum can be calculated from one analysis of  $\mathcal{N}^*$  instead of  $n \times N$  for  $\mathcal{N}$ .

All these properties are built into the DIANA program and its postprocessor program PPR. In this way amplitude and phase calculations are possible for :

1. arbitrary clock sequences and duty cycles;
2. output sampled during one or multiple timeslots;
3. sample and hold effects ( $\sin x/x$ );
4. aliasing & folding effects (multiband simulation);
5. effect of continuous I/O and S/H or continuous inputs;
6. sensitivity and group delay;
7. noise transfer functions;
8. using the multiplier, summator and delay blocks

the same holds for digital filter structures which, after logic design can also be digitally simulated in mode IV.

Fig. 2c illustrates points 1 to 6. It is the simulated amplitude (dB) for the circuit in Fig. 2a, sampled during both  $C1_1, C1_2$  as a function of frequency (linear scale) and for a clock duty cycle of 50%.

Plotted are :

Curve A : piecewise constant input, no S/H effects  
 Curve B : same but with S/H effects. The zero of  $\sin x/x$  occurs at  $2 f_s$  due to double output phase sampling.

Curve C : continuous input, S/H included (most realistic response).

Curves A' B' and C' are corresponding simulations of the folding effect.

A frequency component  $0.5 f_s < f < f_s$  generates an amplitude  $A_m$  at  $f_s - f$  in the baseband. These calculations are of great importance for the study of antialiasing filter requirements.

This result is computed from the basic unit sample responses in the PPR program. Therefore PPR is a powerful tool for all signal processing calculations with sampled data.

Finally Fig. 2d shows the result of sensitivity calculations for Fig. 2a.

Shown is the sensitivity, to capacitor  $C_1$ , of the amplitude of the transfer function for a piecewise constant input sampled during both  $C1_1$  and  $C1_2$ . The output is also sampled during both phases. The sensitivity is calculated from  $1/512$  to  $1/2$  the sample frequency. It has been calculated using the adjoint network concept.

#### SUMMARY

Based on the MNA and adjoint network theory of S.C. networks and the use of macromodels for sampled data building blocks efficient time, frequency sensitivity and noise simulation is possible. By combining this with mixed mode simulation in the DIANA program full sampled data simulation from concept down to transistor level is possible within the same program, using the same language.

#### REFERENCES

- 1 De Man, H., Newton, R., "Hybrid simulation", Proceedings of 1979 ISCAS Conference, July 17-19, Tokyo, Japan, pp. 245-252.
- 2 De Man, H., Rabaey, J., Arnout, G., Vandewalle J., "Practical implementations of a general CAD technique for switched capacitor circuits", IEEE Journ. of Solid State Circuits, SC-15, No. 2, April 1980.
- 3 Vandewalle, J., De Man, H., Rabaey, J., "Time, frequency and z-domain modified nodal analysis of switched capacitor networks", submitted to IEEE Trans. on CAS.
- 4 Vandewalle, J., De Man, H., Rabaey, J., "The adjoint switched capacitor network and its applications", this conference ISCAS 1980.

DIANA PROGRAM

MODE	PRIMITIVES	VARIABLES	ANALYSIS
I) SAMPLED-DATA		V, Q, t, w	TIME (LIN. & NONLIN.) FREQUENCY SENSITIVITY NOISE (ROUND OFF)
II) (SUB) CIRCUIT		V, I, t	TIME, DC
III) TIMING		V, I, t	TIME
IV) LOGIC	(N)AND; (N)OR; (N)EXOR; AOI; OAI; J-K FF & MACRO'S	I, 0, X, U, D, t	TIME

Fig. 1 : Different modes of simulation and primitives available in DIANA. Modes II, III and IV can be mixed.

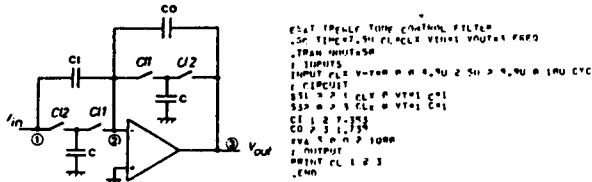


FIG 2a

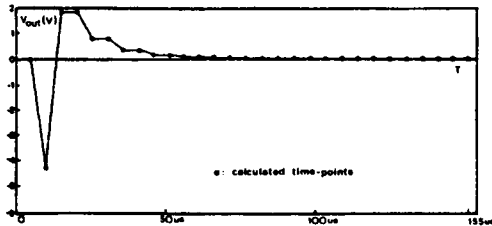


FIG 2b

Fig. 2a : example and its coding.

Fig. 2b : impulse response mode 1.

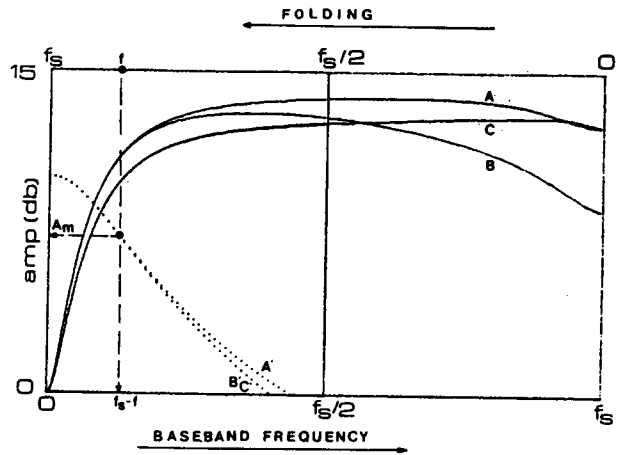


Fig 2c

Fig. 2c : simulated frequency response including folding effects.

Fig. 2d : amplitude density as a function of frequency to capacitor C<sub>1</sub>.

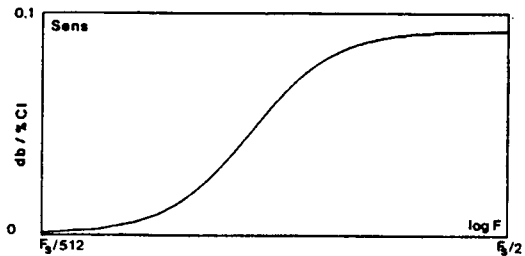


Fig 2d

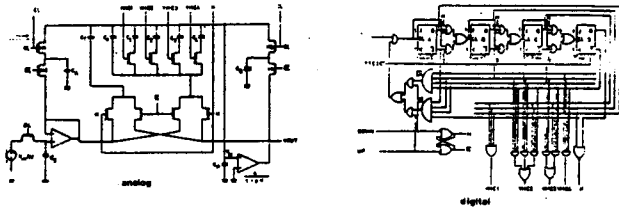


FIG 3<sub>a</sub>

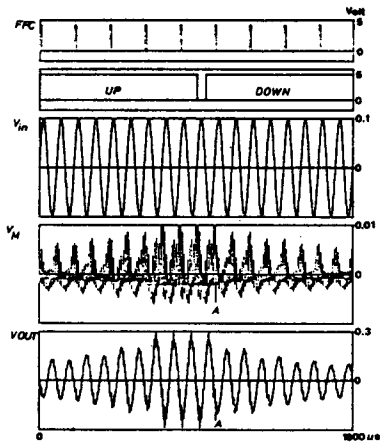


FIG 3<sub>b</sub>

Fig. 3 : Mixed mode simulation of the filter in Fig. 2a including digital part. 1800 time points, 1  $\mu$ s 120 sec CPU, IBM 370-158. Notice spike A resulting from influence of control logic on analog circuit.

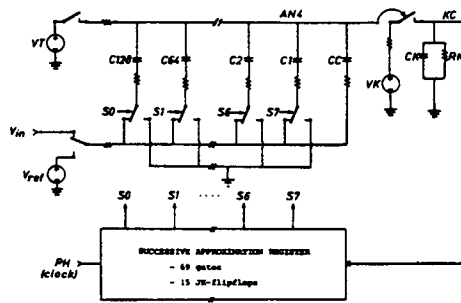


Fig. 4a. 8 bit A/D converter.

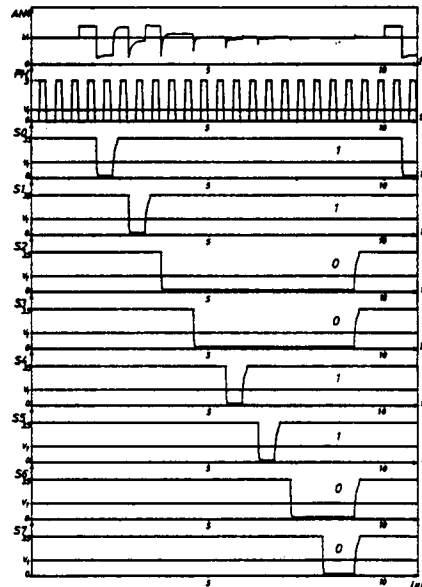


Fig. 4b. Simulation of 8 bit A/D converter; 8,3 sec CPU IBM 3033 600 time steps.