For some time it has seemed likely that the quaternary $In_{1-x}Ga_xP_{1-z}As_z$, which is a direct-gap material extending from the yellow-green to the infrared, might be a better choice of alloy III-V semiconductor to employ for high-energy laser emission (yellow) than $In_{1-x}Ga_xP$. This possibility is inherent in the fact that any increase Δx in Ga composition x that shrinks the crystal lattice can be balanced by a corresponding increase Δz in As composition z that increases the lattice constant, thus leading to a fixed lattice constant *and above all* a mechanism to minimize lattice defects and strains. Utilizing these notions and the usual slider-boat LPE crystal growth process, we have fabricated $In_{1-x}'Ga_x'P_{1-z}'As_z'/In_{1-x}Ga_xP_{1-z}As_z/In_{1-x}'Ga_x'P_{1-x}'As_z'$ ($x' \sim 0.66, z' \sim 0.005; x \sim 0.71, z \sim 0.10$) double heterojunction laser diodes that operate in the *yellow* at current densities ($J < 10^4$ A/cm^2, $\lambda \sim 5850$ Å, 77 K) an order of magnitude lower than comparable $In_{1-x}Ga_xP$ homojunctions. In this report we describe the lattice-matched LPE quaternary growth process and the quaternary double heterojunction laser diodes and their properties.

IIA-5 Efficient $GaAs_{1-x}Sb_x/Al_yGa_{1-y}As_{1-x}Sb_x$ Double Heterostructure LEDs in the 1-μm Wavelength Region—R. E. Nahory, M. A. Pollack, E. D. Beebe and J. C. DeWinter, Bell Laboratories, Holmdel, N.J. 07733.

We report the liquid-phase expitaxial (LPE) growth, fabrication and operation of efficient double-heterostructure (DH) light emitting diodes (LED's) based on the $GaAs_{1-x}Sb_x/Al_yGa_{1-y}As_{1-x}Sb_x$ alloy system.[1-3] These devices emit in the region of lowest loss of optical fiber transmission lines, at wavelengths around 1 μm and beyond. Similar DH GaAs/AlGaAs LEDs have received attention recently[4,5] as possible sources for fiber systems, but at wavelengths in the more lossy 0.8–0.9-μm region.

The LED reported here consists of six epitaxial layers grown by LPE on a [100], Sn-doped GaAs substrate. Three layers of $GaAs_{1-x}Sb_x$, with $x = 0.025$, 0.058, and 0.093, are used between the substrate and subsequent layers to provide stepwise compositional grading.[6] The recombination region of the structure is a layer of $GaAs_{1-x}Sb_x$:Ge ($x = 0.12$) sandwiched between p- and n-type cladding layers of $Al_yGa_{1-y}As_{1-x}Sb_x$ ($x = 0.12, y = 0.17$) to provide confinement. For purposes of comparison, $GaAs_{1-x}Sb_x$ homojunction diodes ($x = 0.12$) were also grown using the same LPE growth system.

Junction edge electroluminescence spectra of the homojunctions peak at 1.04 μm and have a FWHM of 0.06 μm. The external quantum efficiency is ~0.12 percent. For the double heterostructures the spectra are narrower, FWHM as small as 0.043 μm, and peak at ≈1.00 μm. This wavelength differs from that of the homojunctions because of the carryover of a small amount of Al from the n-AlGaAsSb solution during the growth process. The external quantum efficiency achieved for the DH LEDs is 2.1 percent. This corresponds to a power efficiency of 1.9 percent, at a pulsed current level of 0.2 A.

Although the parameters have not yet been completely optimized for these DH LED's, their excellent efficiency in the 1-μm wavelength region makes them strong candidates for use with fiber transmission lines.

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[4] C. A. Burrus and B. I. Miller, *Optics Commun.*, vol. 4, p. 307, 1971.

[5] M. Ettenberg, H. F. Lockwood, J. P. Wittke, and H. Kressel, *IEDM Tech. Dig.*, p. 317, 1973.

[6] R. E. Nahory, M. A. Pollack, and J. C. DeWinter, *Appl. Phys. Lett.*, vol. 25, p. 146, 1974.

IIA-6 Graded Gap Diodes-Increasing the Efficiency of p-n Junction Zinc Sulfo-selenide LED's—R. J. Robinson, T. Martin, and E. Maryniak, Zenith Radio Corp., Chicago, Ill. 60639.

A technique has recently been discussed[1] by one of us for generating at least 10^{17} holes/cm^3 at room temperature in zinc selenide and zinc sulfoselenide from a new type of shallow acceptor level. p-n junction LED's are made by diffusing selected Group IIIa elements (in the presence of zinc) into n-type selenide and zinc sulfo-selenide substrates. Light, however, is generated only on the n-side of the LED; hence only the holes are useful as minority carriers. The p-n junction is placed in a graded-bandgap layer to enhance hole injection: this is necessary because hole mobilities are very low compared to that of electrons. This has resulted in LED efficiencies above one percent. The graded-bandgap layer is produced by low temperature vapor phase epitaxy followed by heating. The technique and efficiency results will be discussed.

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[1] Presented at *Specialist Conf. on Technology of Electroluminescent Diodes*, Atlanta, Ga., Nov. 20–21, 1974. Submitted for publication *Appl. Phys. Lett.*

IIA-7 Guided-Light Beam Deflection/Switching and Modulation Using Tilted-Electrode Structures in $LiNbO_3$ Waveguides—C. S. Tsai and P. Saunier, Department of Electrical Engineering, Carnegie-Mellon University, Pittsburgh, Pa. 15213.

Theoretical and experimental results on new guided-wave electrooptic devices for ultrafast optical deflection, switching and modulation are presented. The devices utilize simple electrode arrangements consisting of a small number of tilted electrodes which effectively simulate prism structures in electrooptic waveguides. Devices using single-mode Y-cut $LiNbO_3$ out-diffused waveguides have demonstrated excellent performance figures: nine beam positions (channels) per unit at a driving voltage of 8 V per beam position, 0.5 dB optical insertion loss, and crosstalks between adjacent channels varying from −13.5 to −9 dB. The new devices are shown to be capable of performing optical multiport beam deflection/switching and modulation at very low driving voltages and at ultrafast speeds because of their very small capacitances, and are, therefore, highly useful for future wideband fiber and integrated optic systems.

Session IIB

Charge-Coupled Devices

IIB-1 Noise Measurements on Buried-Channel Charge-Coupled Devices—R. W. Brodersen and S. P. Emmons, Texas Instruments Incorporated, Dallas, Tex. 75222.

For the first time, measurements of bulk state trapping noise will be reported. These measurements were made on linear 150 stage buried-channel charge-coupled devices (BCCD's). The total device noise was found to be composed of three components; the electrical insertion of signal charge, bulk state trapping, and the output amplifier. We did not observe any of the extraneous parasitic noise sources such as pulser noise and abnormally high input noise which have been observed by previous authors.[1,2]

In making these measurements the concept of correlated double sampling[3] was used in an output amplifier which had a noise level which was equivalent to less than 30 noise electrons. The dominant noise contributors in this amplifier will be discussed.

A low noise input structure for electrical insertion of signal charge was used which introduced a noise equivalent to less than 40 e$^-$. A description of this input will be given as well as an analysis of its operation.

The extremely low noise levels just described which were obtained at the input and output have made possible direct measurement of

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[1] J. E. Carnes *et al.*, "Measurements of noise in charge-coupled devices," *RCA Rev.*, vol. 34, Dec. 1973, p. 553.

[2] A. M. Mohsen and M. F. Tompsett, "The effect of the device on the performance of bulk channel charge-coupled devices," *IEEE Trans. Electron Devices*, vol. ED-21, pp. 701–711, Nov. 1974.

[3] M. H. White *et al.*, "Characterization of surface channel CCD image arrays at low light levels," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 1–10, Feb. 1974.

the noise due to bulk state trapping. In fact, even for very high quality devices (transfer efficiency >0.99999) because of the advances made in reducing the input and output noise, the dominant noise source was due to the bulk states. The spectral density of the bulk state noise will be presented as a function of frequency and signal level. The results will be correlated with transfer efficiency measurements and theory.

IIB-2 A New Method to Measure Very Low Bulk Trap Densities in Silicon

—M. G. Collet, Philips Research Laboratories, Eindhoven, The Netherlands.

The charge transfer efficiency of bulk charge coupled devices (BCCD's)[1] can be degraded by the presence of very low concentrations (10^{10} cm^{-3}) of bulk traps. Measurements on BCCDs yield information about the traps.[2] These measurements and the processing of the devices demand a great deal of time. We therefore tried to device a simpler method for investigating traps that may degrade the BCCD performance.

The n-type slice or epitaxial layer which is to be investigated is almost completely depleted of electrons by means of a reverse bias applied to a p-n junction on the back face and another applied to a p-n junction or a MOS gate on top of the sample. Between the two depletion layers, a narrow conductive channel is left, whose conductivity is kept constant by means of a feedback loop which adjusts the gate voltage. When depletion of the top layer is induced, traps present in that layer start to empty. This emptying process was studied by recording the gate voltage changes necessary to keep the channel conductivity constant. The magnitude of this voltage change yields the trap concentration, while time constant versus temperature measurements yield trap energy level.

The magnitude of the voltage change is proportional to the square of the thickness of the depletion layer, so that very high sensitivity is possible. Experimental results will be shown in which the detection limit was 10^9 cm^{-3}. In all samples examined up till now, two or more types of trap occurred with concentration of at least 10^{10} cm^{-3}.

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[1] L. J. M. Esser, M. G. Collet, and J. G. van Santen, presented at the IEDM, Washington, 1973.

[2] A. M. Mohsen and M. F. Tompsett, "The effect of the device on the performance of bulk channel charge-coupled devices," *IEEE Electron Devices*, vol. ED-21, pp. 701–711, Nov. 1974.

IIB-3 Frequency Response of the Floating Diffusion Input[1]

—S. P. Emmons, D. D. Buss, R. W. Brodersen, C. R. Hewes, Texas Instruments Inc., Dallas, Tex. 75222.

An analysis is presented of the small-signal frequency response of the floating diffusion (FD) input[2] which predicts a band-limiting effect approaching the $\sin x/x$ response of an ideal integrator. The analysis applies with equal validity to all inputs using the potential equilibration technique.[2–4]

This bandlimiting effect is particularly important in signal processing applications because the CCD is inherently a sample-data device. It follows that preservation of signal-to-noise ratio requires that the noise on the processed signal be band-limited to avoid aliasing. In many applications, particularly those involving integration of pre-CCD electronics onto the CCD monolith, it is desirable that this low-pass filtering be accomplished by the CCD input itself. The analysis of the small-signal frequency response of the FD input predicts excellent noise antialiasing under practical conditions of operation which maintain the insensitivity to threshold voltage inherent in this input.

Frequency response data is presented together with noise measurements which agree well with theory.

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[1] This work originally supported by Night Vision Laboratory under Contract DAAK-73-C-0194. More recent work supported by Air Force Avionic Laboratory under Contract F33615-74-C-1054.

[2] S. P. Emmons and D. D. Buss, presented at the Device Research Conference, Boulder, Colo., 1973.

[3] M. F. Tompsett and E. J. Zimany, Jr., "Use of charge-coupled devices for delaying analog signals," *IEEE J. Solid-State Circuits*, vol. SC-8, pp. 151–155, Mar. 1973.

[4] J. E. Carnes, W. F. Kosonocky, and P. A. Levine, *RCA Rev.*, vol. 34, Dec. 1973.

IIB-4 Performance of Multichannel CCD Structure in Filter Applications

—A. A. Ibrahim, Bell-Northern Research, Ottawa, Ont., Canada and M. S. Sabri, Department of Electrical Engineering, University of Ottawa, Ottawa, Ont., Canada.

The implementation of CCD's for transversal filters has been discussed[1,2]. The specific fixed tap weights could be achieved by external resistors which provide the flexibility of implementing different types of filter functions.[1] On the other hand, fixed tap values can be obtained on the chip by using the split electrode technique.[2]

In this paper, a new approach to design of a CCD transversal filter structure is described and the performance is also compared with the simulated results. The approach could be used for on-chip fixed tap weight filter circuits.

The proposed multichannel CCD structure incorporates the two level polysilicon gate technology. It consists of 32 parallel channels having a common input and clock line and separate on-chip output preamplifiers. The delays of each channel vary from 1 to 32 bits with increments of 1-bit delay.

The structure has been used to implement a bandpass filter in the audio frequency range. The CCD was clocked at variable frequencies to achieve different characteristics. The external tap weights were obtained by using variable resistors. The implemented designs had rejection in the stop band greater than 50 dB, ripples in the pass band less than 1 dB and distortion less than 50 dB.

The structure is proposed to fabricate on-chip fixed tap transversal filters.

The design concepts, operating parameters and performance will be presented.

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[1] A. A. Ibrahim, L. Sellars, T. Foxall, and W. Steenaart, "CCD's for transversal filter application," *1974 IEDM Dig.*, pp. 240–243.

[2] D. Buss, *et al.*, "Transversal filtering using charge transfer devices," *IEEE J. Solid-State Circuits*, vol. SC-8, pp. 138–146, Apr. 1973.

[3] J. McLellan *et al.*, "A computer program for designing optimum FIR linear phase digital filters," *IEEE Trans. on Audio and Electroacoustics*, vol. AV-21, No. 6, Dec. 1973.

IIB-5 Fabrication and Operation of Small E-Beam Defined CCD's

—D. A. Robinson, J. B. Barton, T. G. Blocker, D. W. Mueller, and D. R. Collins, Texas Instruments Inc., Dallas, Tex. 75222.

Present trends are toward increased packing densities in LSI MOS and bipolar devices, both for improved circuit performance and lower costs. In particular, CCD structures with high bit densities can provide unique performance in high resolution imaging and in memory applications. E-beam and X-ray lithography can provide finer dimensional capability for microfabrication; however, new processing techniques must be developed which are compatible both with the e-beam or X-ray resists and with the finer dimensional tolerances.

This paper presents data on 4-phase 178-bit linear shift registers with 6.8-μm bit lengths, fabricated using e-beam lithography. Included are devices with 5-μm, 10-μm, and 40-μm channel widths. The 5×6.8-μm bit size represents an increase in bit density of approximately 15 over present conventional CCD shift registers.

This paper will concentrate on the different fabricational techniques required to build a CCD with the increased tolerances involved. The device was fabricated as a surface channel CCD with a four-phase double-level metallization (Al-Al$_2$O$_3$-Al) structure. Each electrode was 1.7 μm in length with varying channel width to 5 μm. All patterning of the device was achieved using an e-beam pattern generator and e-beam resist. In order to maintain narrow channel widths and small diodes, all doping of the substrate was performed