

the noise due to bulk state trapping. In fact, even for very high quality devices (transfer efficiency >0.99999) because of the advances made in reducing the input and output noise, the dominant noise source was due to the bulk states. The spectral density of the bulk state noise will be presented as a function of frequency and signal level. The results will be correlated with transfer efficiency measurements and theory.

IIB-2 A New Method to Measure Very Low Bulk Trap Densities in Silicon—M. G. Collet, Philips Research Laboratories, Eindhoven, The Netherlands.

The charge transfer efficiency of bulk charge coupled devices (BCCD's)¹ can be degraded by the presence of very low concentrations (10^{10} cm⁻³) of bulk traps. Measurements on BCCDs yield information about the traps.² These measurements and the processing of the devices demand a great deal of time. We therefore tried to devise a simpler method for investigating traps that may degrade the BCCD performance.

The n-type slice or epitaxial layer which is to be investigated is almost completely depleted of electrons by means of a reverse bias applied to a p-n junction on the back face and another applied to a p-n junction or a MOS gate on top of the sample. Between the two depletion layers, a narrow conductive channel is left, whose conductivity is kept constant by means of a feedback loop which adjusts the gate voltage. When depletion of the top layer is induced, traps present in that layer start to empty. This emptying process was studied by recording the gate voltage changes necessary to keep the channel conductivity constant. The magnitude of this voltage change yields the trap concentration, while time constant versus temperature measurements yield trap energy level.

The magnitude of the voltage change is proportional to the square of the thickness of the depletion layer, so that very high sensitivity is possible. Experimental results will be shown in which the detection limit was 10^9 cm⁻³. In all samples examined up till now, two or more types of trap occurred with concentration of at least 10^{10} cm⁻³.

¹ L. J. M. Esser, M. G. Collet, and J. G. van Santen, presented at the IEDM, Washington, 1973.

² A. M. Mohsen and M. F. Tompsett, "The effect of the device on the performance of bulk channel charge-coupled devices," *IEEE Electron Devices*, vol. ED-21, pp. 701-711, Nov. 1974.

IIB-3 Frequency Response of the Floating Diffusion Input—S. P. Emmons, D. D. Buss, R. W. Brodersen, C. R. Hewes, Texas Instruments Inc., Dallas, Tex. 75222.

An analysis is presented of the small-signal frequency response of the floating diffusion (FD) input² which predicts a band-limiting effect approaching the $\sin x/x$ response of an ideal integrator. The analysis applies with equal validity to all inputs using the potential equilibration technique.²⁻⁴

This bandlimiting effect is particularly important in signal processing applications because the CCD is inherently a sample-data device. It follows that preservation of signal-to-noise ratio requires that the noise on the processed signal be band-limited to avoid aliasing. In many applications, particularly those involving integration of pre-CCD electronics onto the CCD monolith, it is desirable that this low-pass filtering be accomplished by the CCD input itself. The analysis of the small-signal frequency response of the FD input

¹ This work originally supported by Night Vision Laboratory under Contract DAAK-73-C-0194. More recent work supported by Air Force Avionic Laboratory under Contract F33615-74-C-1054.

² S. P. Emmons and D. D. Buss, presented at the Device Research Conference, Boulder, Colo., 1973.

³ M. F. Tompsett and E. J. Zimany, Jr., "Use of charge-coupled devices for delaying analog signals," *IEEE J. Solid-State Circuits*, vol. SC-8, pp. 151-155, Mar. 1973.

⁴ J. E. Carnes, W. F. Kosonocky, and P. A. Levine, *RCA Rev.*, vol. 34, Dec. 1973.

predicts excellent noise antialiasing under practical conditions of operation which maintain the insensitivity to threshold voltage inherent in this input.

Frequency response data is presented together with noise measurements which agree well with theory.

IIB-4 Performance of Multichannel CCD Structure in Filter Applications—A. A. Ibrahim, Bell-Northern Research, Ottawa, Ont., Canada and M. S. Sabri, Department of Electrical Engineering, University of Ottawa, Ottawa, Ont., Canada.

The implementation of CCD's for transversal filters has been discussed^{1,2}. The specific fixed tap weights could be achieved by external resistors which provide the flexibility of implementing different types of filter functions.¹ On the other hand, fixed tap values can be obtained on the chip by using the split electrode technique.²

In this paper, a new approach to design of a CCD transversal filter structure is described and the performance is also compared with the simulated results. The approach could be used for on-chip fixed tap weight filter circuits.

The proposed multichannel CCD structure incorporates the two level polysilicon gate technology. It consists of 32 parallel channels having a common input and clock line and separate on-chip output preamplifiers. The delays of each channel vary from 1 to 32 bits with increments of 1-bit delay.

The structure has been used to implement a bandpass filter in the audio frequency range. The CCD was clocked at variable frequencies to achieve different characteristics. The external tap weights were obtained by using variable resistors. The implemented designs had rejection in the stop band greater than 50 dB, ripples in the pass band less than 1 dB and distortion less than 50 dB.

The structure is proposed to fabricate on-chip fixed tap transversal filters.

The design concepts, operating parameters and performance will be presented.

¹ A. A. Ibrahim, L. Sellars, T. Foxall, and W. Steenaart, "CCD's for transversal filter application," *1974 IEDM Dig.*, pp. 240-243.

² D. Buss, et al., "Transversal filtering using charge transfer devices," *IEEE J. Solid-State Circuits*, vol. SC-8, pp. 138-146, Apr. 1973.

³ J. McLellan et al., "A computer program for designing optimum FIR linear phase digital filters," *IEEE Trans. on Audio and Electroacoustics*, vol. AV-21, No. 6, Dec. 1973.

IIB-5 Fabrication and Operation of Small E-Beam Defined CCD's—D. A. Robinson, J. B. Barton, T. G. Blocker, D. W. Mueller, and D. R. Collins, Texas Instruments Inc., Dallas, Tex. 75222.

Present trends are toward increased packing densities in LSI MOS and bipolar devices, both for improved circuit performance and lower costs. In particular, CCD structures with high bit densities can provide unique performance in high resolution imaging and in memory applications. E-beam and X-ray lithography can provide finer dimensional capability for microfabrication; however, new processing techniques must be developed which are compatible both with the e-beam or X-ray resists and with the finer dimensional tolerances.

This paper presents data on 4-phase 178-bit linear shift registers with 6.8- μ m bit lengths, fabricated using e-beam lithography. Included are devices with 5- μ m, 10- μ m, and 40- μ m channel widths. The 5 \times 6.8- μ m bit size represents an increase in bit density of approximately 15 over present conventional CCD shift registers.

This paper will concentrate on the different fabrication techniques required to build a CCD with the increased tolerances involved. The device was fabricated as a surface channel CCD with a four-phase double-level metallization (Al-Al₂O₃-Al) structure. Each electrode was 1.7 μ m in length with varying channel width to 5 μ m. All patterning of the device was achieved using an e-beam pattern generator and e-beam resist. In order to maintain narrow channel widths and small diodes, all doping of the substrate was performed