Digest, 746, 1980.
[2]K. W. Gurtler, *IEEE Trans. Electron Devices*, vol. ED-15(12), 980, 1968.

provided breakdown is the only consideration.

IVB-2 Characterization of Tunneling in Ultra-Thin Oxide MOS Devices

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Experimental studies have been carried out to investigate the fundamental limitations on scaling the feature size in MOS technology. Previous theoretical analysis[1] on scaled MOS transistors have predicted that the minimum oxide thickness is 50Å, due to the onset of gate currents. Using standard growth techniques we have fabricated silicon dioxide as thin as 43Å and have fully characterized the gate currents. Our results indicate that oxides that are even thinner than these can be used.

Oxide currents versus gate biases were measured with electrometers on MOS capacitors made with aluminum-gate (t_{ox} = 115Å), N+ polysilicon-gate (t_{ox} = 63Å, t_{ox} = 43Å) on N and P substrates. Experimental data were curve-fitted against the classical Fowler-Nordheim tunnel equation,[2] containing image-force barrier and lowering and temperature corrections, with the effective mass as the only unknown parameter. Oxide thicknesses were experimentally determined from capacitance-voltage and ellipsometry measurements. Using published data on the values for zero-bias barrier heights, an effective mass coefficient of value 0.6 was found to fit the data over four to five orders of magnitudes in current.

Our experimental res[illegible] [illegible] [illegible]at tunneling currents become comparable to the typical junction leakage currents (10 nA/cm^2) at V_g = 3.0V for t_{ox} = 43Å and V_g = 4.2V for t_{ox} = 63Å, respectively. Preliminary reliability study also indicates that the total number of charges flowing through oxide before break-down ranges up to 30 coulombs/cm^2. Therefore, a device lifetime up to 100 years may be expected under the above (relative large) voltages, provided breakdown is the only consideration.

Another important problem at these oxide thicknesses is the depletion regions which form at the polysilicon-oxide interfaces. In the polysilicon gates are depletion regions on the order of 50Å. The width of these depletion regions is found to be described by standard MOS theory. The presence of this thin depletion region in polysilicon not only modifies the tunneling I-V relationship, but is a parasitic series capacitor which reduces the effective gate capacitance. This effect significantly degrades the transconductances of thin-oxide MOS transistors.

Further work in the characterization of oxides as thin as 30Å on MOS capacitors and transistors will be reported at the conference. I would like to acknowledge the many helpful discussions with Profs. Cheming Hu and William G. Oldham.

[1]K. N. Ratnakumar, J. D. Meindl, and D. Bartelink, "Performance Limits of E/D NMOS VLSI," *ISSCC Digest of Technical Papers*, pp. 74-75, Feb., 1980.
[2]M. Lenzinger and E. H. Snow, "Fowler-Nordheim Tunneling into Thermally Grown SiO_2," *Journal of Applied Physics*, vol. 40, No. 1, pp. 278-283, Jan., 1969.
[3]Mong-Song Liang, U. C. Berkeley; private communication.

IVB-3 Fowler-Nordheim Tunneling in MIS Structures

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The objective of this work is to establish a deeper understanding of the Fowler-Nordheim electron tunneling from silicon dioxide.

Despite the extensive theoretical and experimental attention given to Fowler-Nordheim tunneling in MIS structures, there is very little agreement between various experimental and theoretical results.[1] This suggests the need for a careful and thorough analysis that takes into account more of the