

It has been shown in this work that the extra tunnel component is due to electron tunneling from the Si valence band [9], rather than hole transport through the oxide [6,10] or photogeneration of hole-electron pairs in the Si.

Conduction in thin dielectric layers is presently being studied in various areas, such as erasable non-volatile memories, charge loss in dynamic RAMS, and reliability of advanced scaled-down MOS technology. The results and interpretation presented in this work are useful for understanding of conduction mechanisms in the above applications.

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IIB-2 Direct Tunneling in Thin Gate-Oxide MOS Structure—Chi Chang, Robert W. Brodersen, Mong-Song Liang and Chenwing Hu, Department of Electrical Engineering and Computer Science, Electronic Research Laboratory, University of California, Berkeley, CA 94720, (415) 642-1094.

This work is aimed at both the theoretical understanding and experimental characterizations of charge tunneling in thin-oxide MOS structures at relative low voltage regime.

Electron tunneling through thin oxides (<150Å) is being used for programming and

erasing memory cells in EEPROMs. In this application, high current density ($>1\text{mA}/\text{cm}^2$) is passed through the thin oxide by means of large oxide voltages and high electric fields ($>10\text{MV}/\text{cm}$). This mechanism generally makes use of Fowler-Nordheim (F-N) tunneling and has been studied extensively [1,2]. On the other hand, it is also very important to understand the tunneling current behavior in the "direct" tunneling regime where the oxide voltage is comparable to or less than the oxide-semiconductor barrier height ($\sim 3.2\text{eV}$). Direct tunneling can be encountered during the read cycles of memory cells resulting in leakage currents which can directly affect the memory cell charge retention. Also, direct tunneling will become increasingly important as MOSFETs are scaled into the sub-micron regime. This gate leakage current can cause device characteristics to change as a result of interface-state generation and oxide charge trapping.

We have used the classical free-electron tunneling theory with a Franz-type two-band as well as a parabolic one-band dispersion relation in the WKB approximation to calculate the tunneling current in MOS structures for charge injections from the gate and Si-substrate. We shall show that both these tunneling theories predict the current-voltage behavior quite satisfactorily in the F-N regime for oxide thicknesses ranging from 30Å-150Å. However, by comparing with experimental data, we have found that in the direct tunneling regime (an oxide voltage below 3.2V) that the two-band theory provides a more accurate description of the current-voltage behavior than the one-band theory.

Some of the important experimental observations (consistent with our theoretical calculations based on the two-band theory) are: (A) The tunneling current changes much slower as a function of oxide field under "direct" tunneling than under "F-N" tunneling. This is primarily a consequence of the fact that the oxide barrier is trapezoidal in shape in the "direct" regime where the tunneling probability dependence on oxide voltage is reduced. A secondary reason is that electrons with energies of many kTs below the Fermi level will contribute appreciably to the total current in the "direct" tunneling regime due to the two-band effect. (B) For substrate emission

(+Vg), tunneling by silicon valence-band electrons becomes significant at oxide voltages between $\sim 1.1\text{V}$ and $\sim 3\text{V}$. It disappears below $V_{ox} \sim 1.1\text{V}$ due to the absence of available states in the Si bandgap. (C) For gate emission (-Vg), holes situated at the Si-SiO₂ interface will tunnel out for samples with oxide thickness less than 40Å. This phenomenon is responsible for the substrate "deep depletion" effect observed in the ultra-thin oxide n-type substrate MOS case under low substrate hole generation condition.

These studies will make it possible to develop device design rules for device geometries near the fundamental limits of scaling, and will be very useful in the future design of EEPROMs as these devices are scaled.

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IIB-3 Analysis and Modeling of Floating-Gate E2Prom Cells—A. Kolodny, S. Nieh, B. Eitan and J. Shappir [1], Intel Corp., Santa-Clara, CA 95051, (408) 496-9447.

Floating-gate devices which utilize tunneling through thin dielectric layers are emerging as a major type of electrically-erasable non-volatile memory [1-4]. This work presents a detailed analysis and modeling of write/erase characteristics of such memory cells.

The device under consideration is an n-channel MOS transistor with a floating polysilicon gate. The write/erase path is through thin oxide between the floating gate and the drain [1]. The WRITE operation (charging the floating-gate with electrons) is relatively well understood [5]. The ERASE operation (discharging electrons from the floating gate), involves a high voltage pulse on the drain and is more complicated. This is due to the following effects which have not been discussed previously. (a) *Depletion in the channel*: while the cell is being erased, the floating gate becomes positive. As a result, the channel region under the floating gate goes

into depletion. The back-bias of several volts on this depletion layer reduces the effective capacitance between the floating-gate and the substrate, causing a reduction in the coupling ratio of the cell. (b) *Inversion in the n⁺ region under the tunnel oxide*: an electric field intensity above 10⁷V/cm is required for sufficient tunneling currents; at this field, the n⁺ region beneath the tunnel oxide is inverted. Hence there is an additional voltage drop across the depletion layer in the n⁺ region. For nondegenerate material, this voltage drop is more than the equilibrium value of $2\rho_F$, since thermal equilibrium cannot be reached during the short ERASE operation. The holes in the inversion layer are generated either by avalanche multiplication or band-to-band tunneling in the n⁺ silicon. (c) *Hole flow into the substrate*: a surface channel from the inversion layer in the drain region beneath the tunnel oxide to the substrate might be turned on, allowing flow of holes into the substrate. It is experimentally shown that this effect enhances positive charge trapping in the tunnel oxide, and alters the Fowler-Nordheim characteristic.

This work presents experimental evaluation of these effects, and describes a numerical model that includes them in the simulation of write/erase characteristics. Experimental techniques for measurement of model parameters are discussed. This new device model is useful as tool for the design characterization and optimization of E2PROM cells.

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IIB-4 Analysis of the Channel Inversion Layer Capacitance in the Very Thin-Gate IGFET—Soo-Young Oh, Suk-Gi Choi, C.G. Sodini and J.L. Moll, Hewlett Packard IC Structure Research, 3500 Deer Creek Road, Palo Alto, CA 94304.

As the gate insulator thickness approaches the channel thickness, the gate capacitance is