MOSFET Degradation Due to Stressing of Thin Oxide

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Abstract—Oxide and interface traps in 100 Å SiO_2 created by Fowler-Nordheim tunneling current have been investigated using capacitor *C-V*, *I-V*, and transistor *I-V* measurements. The net oxide trapped charge is initially positive due to hole trapping near the anode interface and, at sufficiently high fluence, it becomes negative due to the trapping of electrons with a centroid of 60 Å from the injector (cathode) interface. Interface traps (Surface states) are created by tunneling electrons flowing to and from the substrate. The interface-trap energy distribution gives a distinct peak at 0.65 eV above the valence band edge. The positive charge trapping and interface traps generation saturate at high electron fluence, but not the electron trap generation. The generation rates for electron traps and interface traps are weak functions of tunneling current density over the range tested. The interface traps cause degradations in subthreshold current slope and surface electron mobility. The threshold-voltage shift can be either positive or negative under the combined influence of the oxide charges and the interface charges.

I. Introduction

FOWLER-Nordheim (F-N) tunneling through thin oxides has been widely used as the mechanism for programming and erasing memory cells in EEPROM's. On the other hand, tunneling can become undesirably significant in an aggressively scaled MOSFET. It has been found that these tunneling currents can lead to oxide charge trapping and interface traps generation [1], [2], which, in turn, cause drift in threshold voltage and degradation of transconductance and has been identified as one of the major reliability problems for EEPROM and scaled MOSFET. Recently, these stabilities in the device characteristics have been studied extensively using bias-temperature aging [3] and high field stressing techniques [4], [5]. Results of these studies indicate that interface and oxide charge trapping are closely linked to the device instabilities. However, a good understanding is still lacking in regard to their individual contributions to the degradation of device characteristics.

The objective of this work, therefore, is to quantitatively characterize the generation of these charges, including both positive and negative oxide trapped charges and interface trapped charges, and to correlate them with the degradations of thin gate MOS transistor characteristics.

II. Devices Preparation

The test devices are arsenic-doped silicon-gate MOS capacitors and silicon gate n-channel transistors fabricated on ⟨100⟩ p-type substrate with doping of $2 \times 10^{15}/cm^3$ and $1.3 \times 10^{17}/cm^3$, respectively. The gate oxides of both devices are approximately 100 Å thick, grown in dry oxygen ambient at 900°C followed by 10 min N_2 annealing at the same temperature. The thickness of the oxide is determined by ellipsometry and checked with low-frequency *C-V* measurement. The capacitors are circular in shape and are 750 μm^2 in area. The transistors have effective channel length of 23 μm, channel width of 25 μm. Contact pads are made of evaporated aluminum. The back surfaces of the samples are also metalized with aluminum. All samples are given a post metallization anneal in forming gas at 450°C for 20 min to obtain good ohmic contact and to reduce interface trap density.

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III. Experimental Techniques

The experimental setup consists basically of three sets of instruments: a) current and voltage sources for oxide stressing, b) meters for F-N *I-V* measurement, and c) quasi-static and 1-MHz MOS *C-V* meter. Each instrument is controlled via a HP 9845 desktop computer, which is also used to log and analyze data. The 1 MHz *C-V*, quasi-static *C-V* and bi-directional *I-V* characteristics (positive and negative bias) are first measured for initial parameters check. The devices are then subjected to *F-N* current stress using a constant current source. After known time intervals, the stressing is interrupted and *C-V* and *I-V* plots are remeasured. This procedure is repeated until device broke down. Typical *I-V* characteristics for a 110-Å gate oxide MOS capacitor before and after stress is shown in Fig. 1. Flat-band voltages (V_{FB}) estimated from 1-MHz *C-V* curves is used as the surface potential integration constant for interface traps extraction from the quasi-static *C-V* plot. For a first-order approximation, charges located at the interfaces have no effect on the *I-V* characteristics (but do affect *C-V* shifts). Trapped bulk oxide charge density and centroid are calculated from bidirectional *I-V* measurements using the simple relations [6]

$$\bar{x} = T_{ox} \cdot \frac{\Delta V_g^+}{\Delta V_g^+ + \Delta V_g^-} \quad (1)$$

$$Q_{ot} = \Delta V_g^+ \cdot \frac{\epsilon_{oz}}{\bar{x}} \quad (2)$$

where ΔV_g^+ and ΔV_g^- are voltage shifts for positive and negative gate bias. Q_{ot} is the net oxide trapped charges, and $\bar{x}$ is the trapped charge centroid measured from the gate. To minimize any undesirable trapping of oxide charges that might take place during *I-V* measurements, the current densities in these measurements are kept at least two order of magnitude lower than the stressing current.

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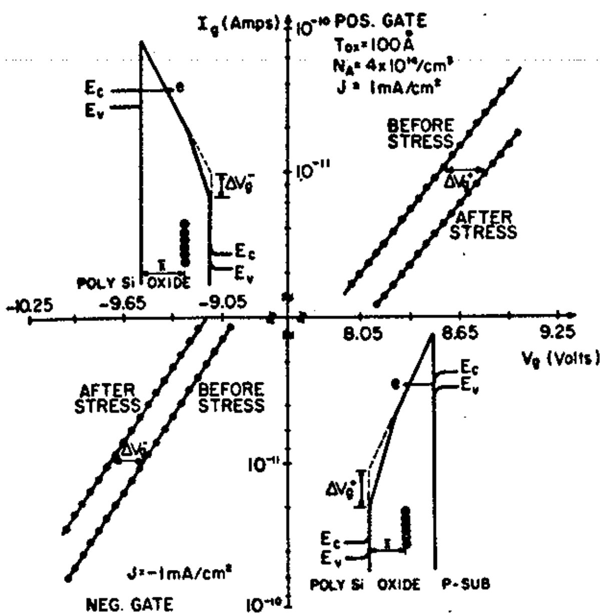

Fig. 1. F-N tunneling I_g-V_g characteristics for ~100 A oxide MOS capacitor before and after current stressing. The insets show the energy band diagrams of a MOS system with oxide trapped charges.

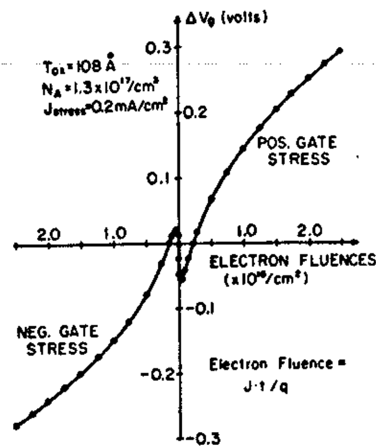

Fig. 2. The change in the gate voltage versus electron fluence under constant current positive and negative gate stressing for ~108-A oxide MOS transistor with source/drain connected to the substrate.

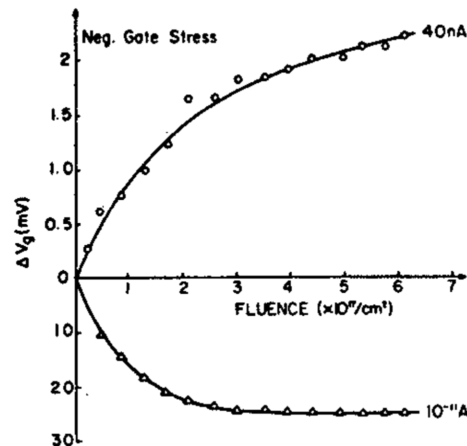

Fig. 3. The change in the gate voltage versus electron fluence under constant current stressing for ~30-A oxide MOS capacitor.

IV. Results and Discussions

A. *Positive Oxide Trapped Charge*

Both positive and negative oxide charges are observed after current stressing of either polarity. The trapping of positive oxide charge during constant current stressing results in a reduction in the gate voltage, whereas any buildup of negative oxide charge is reflected as an increase in the gate voltage. A plot of the change in gate voltage versus electron fluence (number of electrons that have passed through the oxide per unit area) under constant current stress is shown in Fig. 2. It is seen that positive charge trapping dominates during the initial period of current stressing below an electron fluence $\sim 10^{17}/cm^2$. The centroid of the positive charge which is found to be ~10-20 Å away from the anode is measured by the combined *C-V* and *I-V* method [1] at the low fluence. The fact that the voltage shift causes by positive gate stress is always greater than that causes by negative gate stress suggests that the positive charge traps are more abundant near the poly-SiO_2 interface than the substrate-SiO_2 interface. It is also discovered that these positive charges are easily detrapped by reversing gate bias even at gate voltage lower than the stressing voltage. This initial positive charge created by tunneling current was also reported by Itsumi and by Jenq *et al.* [7], [1] by monitoring flatband voltage shifts of H-F *C-V* characteristics.

The appearance of positive charges, we believed, is caused by the hole trapping near the anode valence band edge as a result of the electron-hole pairs generation inside the anode by the tunneling electrons [8]. Electron-hole pair generation near the substrate surface with unity quantum efficiency (number of pair generation per one tunneling electron) by energetic electron tunneling from the gate is indeed observed in 1000-Å oxide MOS structure [9]. The quantum efficiency of tunneling induced pair generation is measured to be between 1 and 2 in our 100-Å oxide sample [10].

To demonstrate the close relationship between pair generation and positive charge build-up, the trapping characteristics of a 30-Å gate oxide MOS capacitor under constant current stress is shown in Fig. 3. For low current stressing (low gate voltage), the energy of tunneling electrons is too low to create measurable pair generations [10] and only electron trapping by pre-existing electron traps is observed as evidenced in the negative ΔV_g. However, for stressing under the applied voltage sufficiently high to cause pair productions (0.9 pairs generated per tunnel electron [10]), positive charge trapping is dominant as evidenced by the positive ΔV_g. The hole traps appear to be pre-existing (rather than continuously generated) as can be seen from the voltage saturation at higher fluence.

The more common mentioned process of impact ionization in the oxide followed by hole trapping at or near the anode [11], [12] is not a probable process in this case in view of the fact only low energy electrons (4 eV < SiO_2 bandgap, 9 eV) in the oxide are involved in the above experiments. The physical origin of hole traps is not clear but we tend to reject the possibility of hole traps due to soft X-ray radiation damage during fabrication because we have observed the same positive gate voltage shifts of three devices having poly-gate electrode with and without metal contact made by thermal, and E-gun evaporation of aluminum. The fact that these charges are

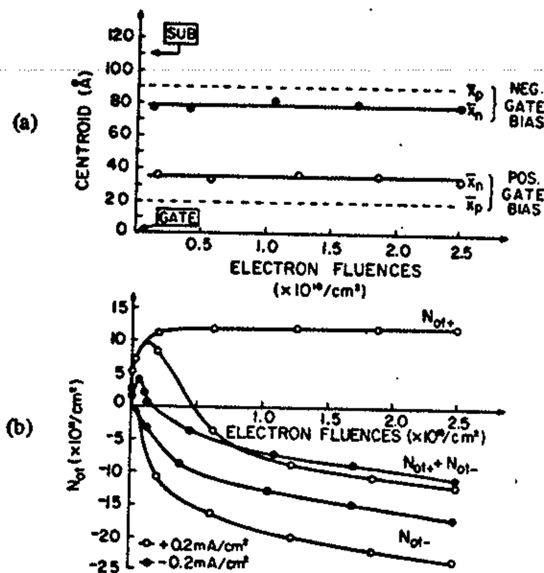

Fig. 4. (a) Extracted negative oxide charge centroid ($\bar{X}_n$) versus electron fluence for positive and negative gate stress by assuming positive charge is 20 A ($\bar{X}_p$) away from the anode. (b) Extracted positive and negative oxide charge densities versus electron fluence for positive and negative gate stress.

relatively unstable is indicative of the close communication between these charges and the anode.

B. Negative Oxide Trapped Charge

At high electron fluences, electron trapping dominates over the initial positive charge trapping. This is easily seen from the positive rising portion of gate voltage change of Fig. 2. Typical plots of extracted oxide charge and charge centroid with fluence are shown in Fig. 4 which are the net effect of the positive and negative oxide charges (Q_{ot+} and Q_{ot-}). The trapping of electrons in the oxide has been reported previously [2], and would not be discussed in any detail except to point out the fact that two processes are involved: the filling of existing traps and the generation of new traps which are subsequently filled by electrons. The centroid of the trapped electrons is ~60 Å from the injector interface.

For the range of oxide fields used in this work, the tunneling distance in the oxide is around 30 Å. After entering the conduction band of the oxide, electrons will gain kinetic energy as they traverse through the remaining portion of the oxide while making collisions with the lattice on their way out. For a typical oxide field of 10 MV/cm, electrons can accelerate up to 30 Å beyond the tunneling exit point and gain an energy of 3 eV or less (due to collisions with longitudinal optical phonons) before reaching the centroid. Therefore, it can be concluded that the energy required to generate an electron trap in the oxide is 3 eV or less. The trap generation rate is a function of the oxide field [13] and is about 10^{-6} at $E_{ox} \sim$ 8-10 MV/cm [2].

C. Generation of Interface Traps

Besides the oxide trapped charges, interface trapped charges at the substrate-SiO_2 interface are also generated during the stress. Fig. 5(a) is a set of *C-V* characteristics of MOS capacitor subjected to positive and negative gate bias stresses, respectively. The interface trap densities extracted by using quasi-static technique [14] are shown in Fig. 5(b). There are several interesting features to be mentioned here: a) The magnitude of the generated interface trap density and distribution are very similar for positive and negative bias stress. b) A peak at ~0.65 eV above valence band edge is seen in all stressed samples together with a background of distributed states across the bandgap. c) For both positive and negative stressings the flat band voltage initially shifts to the negative direction and eventually increases in the positive direction. Positive stressing differes from negative stressing in that the flatband voltage turn-around point appears at much lower fluence. This is because hole trapping is close to the substrate interface for negative gate stressing and is close to the gate interface (and therefore has little effect on V_{FB}) for positive gate stressing.

Interface trap generation processes based on the creation of mobile charge carriers in the bulk of SiO_2 have been proposed [15]. In the stressing processes used here, generated charge species in the bulk of SiO_2, if any, will move in the opposite direction for the two stress polarities and would therefore be expected to produce quite different interface trapped charges. The presence of the discrete state at 0.65 eV above valence band edge has been reported by Shiono *et al.* [1] by temperature-bias (BT) aging of MOS transistors. It is however surprising that they have observed two different discrete states: the 0.65-eV state is seen only under positive gate BT stressing and a different state at approximately 0.3 eV above the valence band edge is observed when the device is subjected to negative gate BT stressing. It is difficult to compare their results with our work since the stress procedures are very different. There is also no indication whether their gate current is significant during BT stressing to attribute the interface traps generation to electron fluence through the interface.

The interface trap density has been measured as a function of stress current and electron fluences. Fig. 6 shows the midgap and peak interface trap density versus electron fluence for different stress current levels. The trap density increases with electron fluence but shows saturation at high fluence. The saturated density level is only a weak function of the stress current density or field. The interface traps are probably pre-existing sites at the interface and the electron fluence merely "exposes" or "activates" these traps by mechanisms such as breakage of energetically favorable Si-H or Si-O bonds at the interface leading to dangling Si bonds at the interface. Since the energy of electrons involved in F-N tunneling is much smaller than UV light and e-beam used in the study of radiation-induced interface traps, it could be expected that the interface trap generation mechansims would be quite different in two cases. For example the well-known mechanism of electron-hole pairs generation and subsequent hole transport and interface trap generation is not likely to occur in the present experiment. It is also not surprising that with the higher energy involved radiation induced interface trap density does not show the presence of the discrete state observed in this experiment.

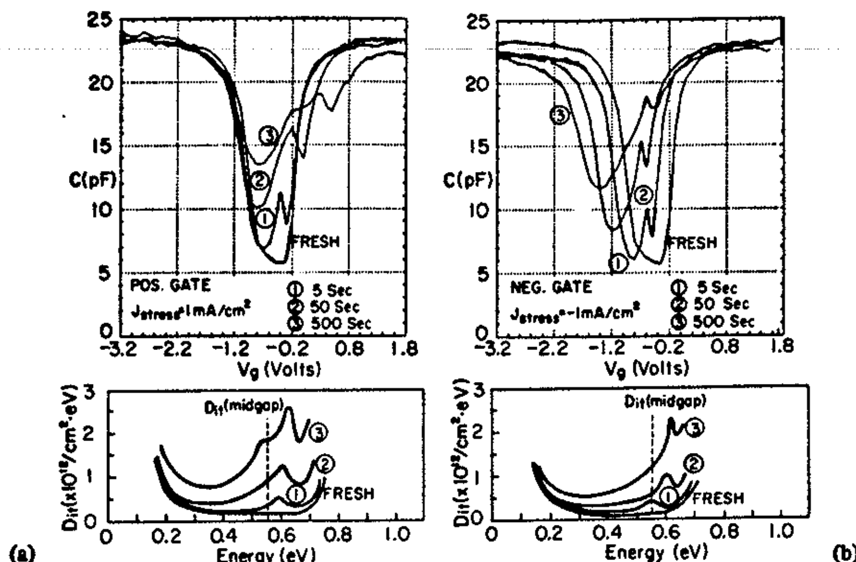

Fig. 5. (a) Quasi-static *C-V* characteristics of MOS capacitor with positive and negative gate stressing, respectively. (b) Interface traps densities extracted from (a).

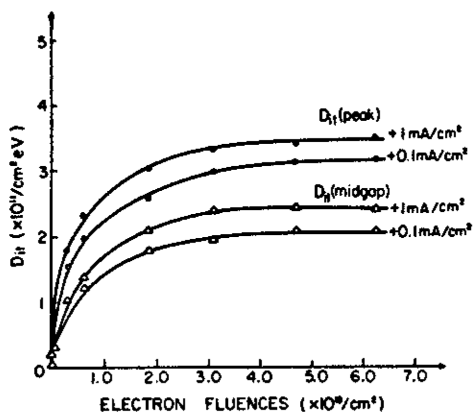

Fig. 6. Midgap and peak interface trap densities versus influence for different stressing current levels.

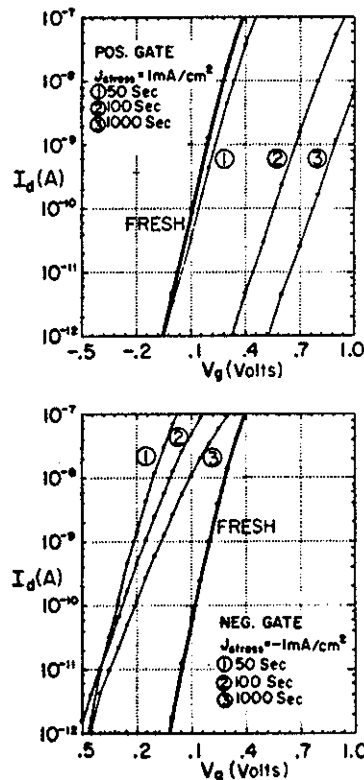

Fig. 7. Subthreshold current versus gate voltage characteristics for positive and negative gate stressing with different fluences.

D. Degradation of Subthreshold Current Slope

The subthreshold current versus gate voltage characteristics for both positive and negative gate stressing with different fluences are plotted in Fig. 7. The slopes of subthreshold currents are seriously degraded by current stressing and are plotted as a function of electron fluence in Fig. 8(a). The interface trap density at ~0.7 eV above valence band edge can be deduced from the subthreshold current slope [16] and it is plotted in Fig. 8(b) together with the density deduced from *C-V* measurement (see Fig. 5(b)). Clearly, the degradation of the current slope is due to the presence and is a unique function of the density of interface traps located close to the conduction band edge independent of stress current level and polarity.

E. Threshold-Voltage Shift

Transistor I_d-V_g plots after positive and negative polarity stressings for different stressing fluences are shown in Fig. 9 (a) and (b), respectively. The large negative V_T shift for negative gate stressing is to the positive charge trapping near the substrate interface. The insensitivity of F-N *I-V* characteristics due to trapped oxide charge close to the interface (the positive charge) offers a simple way to distinguish between the contributions of the trapped oxide charges and interface charges to the threshold voltage shifts (ΔV_T). For positive gate stressing, the measured F-N gate voltage shift (ΔV_g) is due to the net influence of trapped oxide charges as well as the interface charges as presented in Fig. 10(a). Therefore, their difference yields the contribution to the threshold-voltage shift by the interface charges and the amount of these

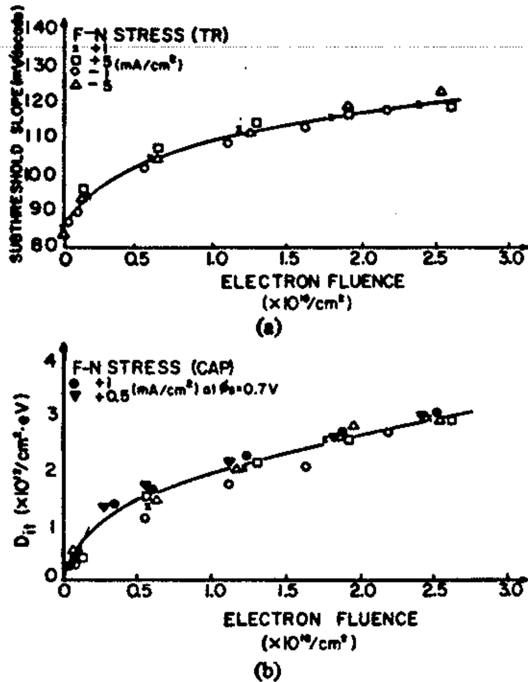

Fig. 8. (a) Subthreshold current slope extracted from Fig. 7 versus electron fluence for different stressing currents. (b) Comparison of deduced D_{it} from Fig. 5(b) versus electron fluence.

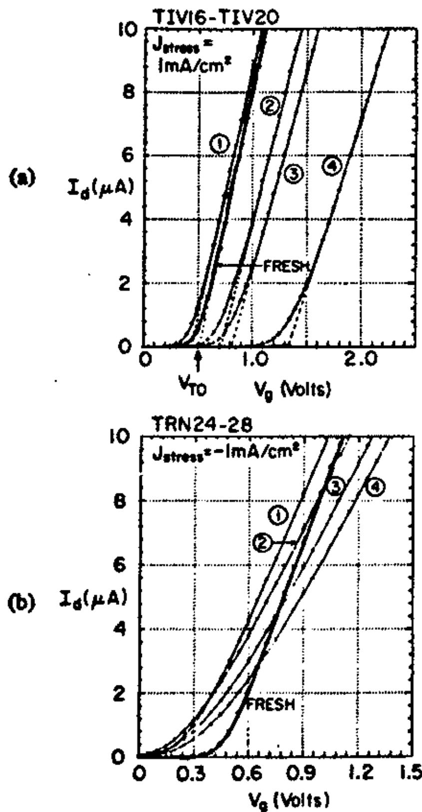

Fig. 9. (a) Transistor linear region (with V_{ds} = 50 mV) I_d-V_g plots for different stressing fluences under positive gate stress. (b) under negative gate stress.

charges is given by

$$Q_{it} = -\frac{\epsilon_{ox}}{T_{ox}} \cdot \Delta V_{Qit} = -\frac{\epsilon_{ox}}{T_{ox}} \cdot (\Delta V_T - \Delta V_g). \tag{3}$$

In the negative gate stressing case, since the positive oxide trapped charge is located near the substrate interface, about

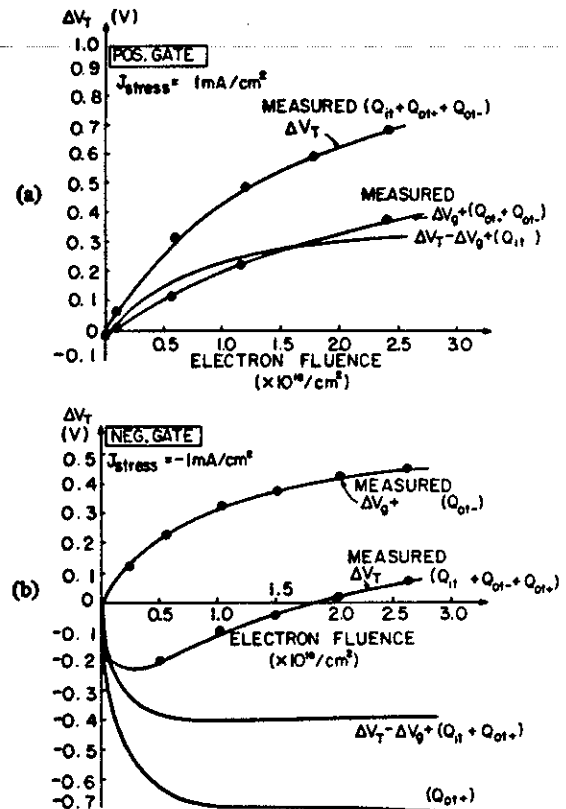

Fig. 10. (a) Measured positive gate stress threshold voltage shift ΔV_T and the contribution from net oxide trapped charges (positive and negative charges), ΔV_g^{+} is the contribution from interface trapped charge. (b) Measured negative gate stress threshold voltage shift ΔV_T and the contribution from negative oxide trapped charge (detail in the text). Contribution of positive oxide trapped charge to the V_T can be deduced by assuming the same interface trapped charge term as positive gate stress case.

10 Å away which is within the tunneling distance of electrons, the "positive" F-N gate voltage shift (ΔV_g^{+}) due to this charge is quite small [17], especially in view of the possibility of temporary charge detrapping during the gate voltage shift measurement itself. By assuming the same interface trap generation rate as in the positive gate stress, we are able to separate the contribution of positive oxide trapped charges from the rest and plot it in the bottom curve in Fig. 10(b). As expected, the influence on the threshold voltage by the positive charges in this case is very significant.

F. Mobility Degradation

The transconductance deduced from transistor I_d versus V_g curve is plotted in Fig. 11 which shows serious degradation after oxide stressing. There is no evidence that the reduction is due to a decrease in inversion layer charge density as stated in [4] rather than true mobility degradation. On the contrary, true mobility degradation due to added scattering from interface trapped charges appears to be responsible for the reduction in transconductance, as discussed below.

The drain current after stressing can be expressed as

$$I_d = \mu_n \frac{W}{L}\left[C_{ox}'(V_g - V_T) - q\int_{2\phi_F}^{\phi_s(V_g)} D_{it}(\Psi)\, d\Psi\right] V_{DS} \tag{4}$$

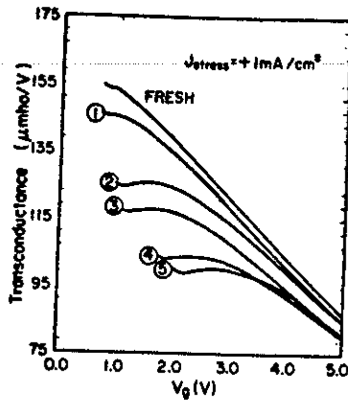

Fig. 11. Transconductance degradation due to the current stressing versus gate voltage for various stressing fluences.

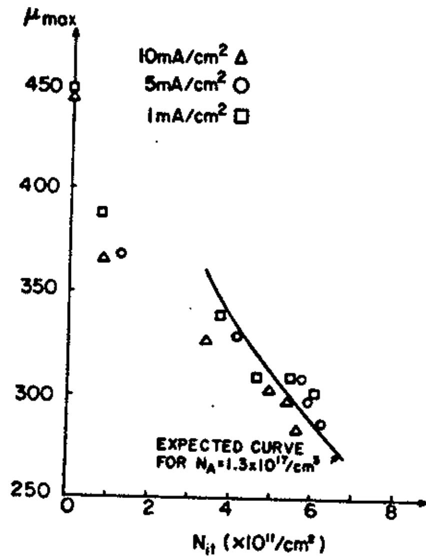

Fig. 12. Maximum effective mobility versus interface trapped charge at threshold condition for various stressing current. The solid curve is the expected true mobility taken from Sun's work [18].

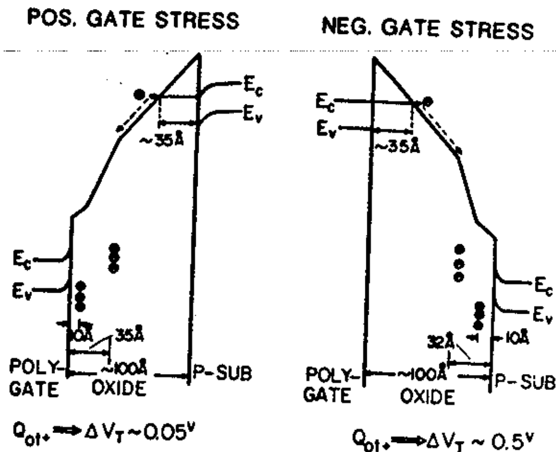

Fig. 13. The locations of oxide trapped charges for positive and negative gate stressings.

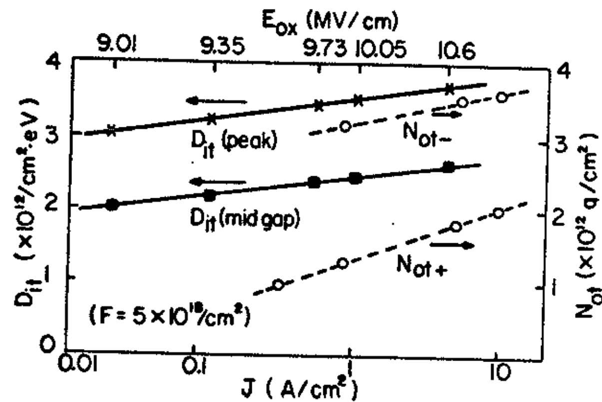

Fig. 14. Peak and midgap interface trap densities, negative oxide trapped charge, and positive oxide trapped charge versus stressing current density for stressing fluence $5 \times 10^{18}/cm^2$.

where the first term in the brackets represents the total channel electron charges (mobile and trapped) and the second term represents the interface trapped charges.

True mobility degradation and reduction of inversion charge can be lumped into so-called effective mobility term and expressed as

$$I_d = \mu_{eff} \frac{W}{L} [C_{ox}'(V_g - V_T)] V_{DS}. \quad (5)$$

The peak effective mobility (corresponding to the peak dc transconductance) against the N_{it} (from Fig. 9 and 3) is plotted in Fig. 12. The solid curve is the expected true mobility taken from Sun's work [18]. The experimental data follows the curve but starts from a lower mobility. This indicates that the transconductance degradation is predominantly caused by the true mobility degradation.

V. Conclusions and Other Discussions

A study of the effect of F-N tunneling current on thin oxide MOS capacitors and transistors has been carried out. It is found that the tunneling current leads to trapping of charges in the oxide as well as generation of interface traps at the SiO_2-substrate interface. The effect of these charges are studied with both MOS capacitors and N-channel transistors.

The trapped charges change from an initial positive charge at low electron fluences to a negative charge at fluence higher than $10^{17}/cm^2$ for both gate biases. The positive charge is located near the anode and the final negative trapped charge is located 30-35 Å from the anode. The interface trap distributions are similar for positive and negative stresses with a discrete state at ~0.65 eV above the valence band edge. The locations of the charge centroids are summarized in Fig. 13. It seems that both electron fluence and the electric field are responsible for the oxide and interface trap generations. The interface and oxide charge trappings versus stressing current density and oxide field are shown in Fig. 14. The strong current dependence of positive charge trapping indicates an increased hole generation and trapping at high current stress.

The stressing current densities used in this study are comparable to those encountered in EEPROM's [19] but much larger than expected for normal transistor operation. It is therefore necessary to know how the degradation varies with current density. For a fixed fluence, interface traps, subthreshold current slope, and effective electron mobility which are shown in Figs. 5, 8, and 11 are rather insensitive to current density. This insensitivity justifies the use of high stressing current density for accelerated tests.

The fluence per year of tunneling and channel hot electron emission versus the gate voltage, oxide thickness, and channel length is shown in Fig. 15. Channel hot-electron emission is

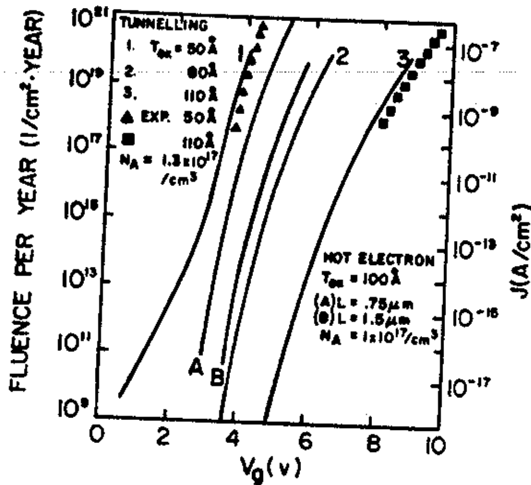

Fig. 15. Fluence per year of tunneling and channel hot-electron emission versus gate voltage, oxide thickness, and channel length.

estimated from a theoretical model [20]. Since no significant degradation is expected until fluence is large than $10^{17}/cm^2$, oxide as thin as 80 Å may be used in 5-V circuits if F-N tunneling is the only source of electron fluence. The channel hot-electron emission, on the other hand, produces very high fluence in a short time. How the impact of hot electron fluence on device degradation differs from the impact of tunneling electron fluence, however, remains to be studied.

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