

Guest Editors' Introduction

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Research over the last decade has enabled high-performance systems such as powerful workstations, sophisticated computer graphics, and multimedia systems such as real-time video and speech recognition. A significant change in the attitude of users is the desire to have access to this computation at any location, without the need to be connected to the wired power source. This has resulted in the explosive growth of research and development in the area of wireless computing over the last five years.

This special issue deals with several key technologies required for wireless computing. The topics covered include reliable wireless protocols, portable terminal design considerations, video coding, RF circuit design issues and tools, display technology, energy efficient application specific and programmable design techniques, energy efficiency metrics, low-voltage process technology and circuit design considerations, and CAD tools for low-power design at all levels of abstraction.

The first three papers deal with low-power wireless terminal design, protocols, and system infrastructure. Agrawal et al., presents a wireless ATM network (SWAN) that provides end-to-end connectivity to mobile end-points equipped with RF transceivers for wireless access. This paper describes the design and implementation of the ATM-based wireless last-hop, including the air-interface control, the MAC, and low-level ATM transport signaling. Chien et al., presents a testbed to evaluate node architectures that support multimedia applications and services across a wireless network. A low bitrate subband video compression algorithm is evaluated for video networking across bandwidth-limited RF channels. Gordon et al., describes the design of a low-power video decompression chipset for portable applications. A error resilient algorithm is used based on subband decomposition and pyramid vector quantization. A variety of power reduction techniques are presented for application specific designs including low-voltage operation, computation vs. memory trade-offs, programmability vs. dedicated hardware, etc.

Chian et al., describes the IC implementation challenges of a 2.4 GHz wireless LAN chipset developed at Harris Semiconductor. The technology considerations, CAD methodology, and the manufacturing considerations are presented. The lessons learned from designing this chipset are presented. Sarma and Akinwande review the flat panel technologies available for portable systems. They review display requirements, and propose metrics to evaluate display technologies. Current day as well as emerging technologies are evaluated.

The Kuroda and Sakurai paper presents some key technology and circuit considerations for low-voltage high-performance system design. They propose a standby power reduction technique where the threshold voltage of the devices are raised to lower idle leakage power. They also propose feedback circuits to adjust the substrate bias to reduce fluctuations in threshold voltage. Burd and Brodersen present techniques for energy efficient programmable processor design. A key contribution in this paper is the definition of energy efficiency metric for various user modes including fixed throughput maximum throughput, and burst throughput modes. Tiwari et al., presents techniques to analyze and optimize power dissipation of software. A measurement based instruction level power analysis approach is used to provide an accurate power cost for software. The ability to model power dissipation of software is key to finding energy efficient programmable implementations.

The final two papers address CAD tool issues for low-power design. Mehra et al., presents various architectural and behavioral approaches for power minimization. A key new idea emphasized involves algorithm partitioning to preserve locality in the assignment of operations to hardware units. This not only reduces implementation area, but

also the number of accesses to high capacitance interconnect. Monteiro and Devadas review power estimation and optimization techniques at the logic level. Simulation-based as well as probabilistic approaches are described for switching activity estimation in sequential circuits. Various power reduction techniques are described including a data dependent logic level power down approach called precomputation.



Anantha P. Chandrakasan received the B.S., M.S., and Ph.D. degrees in Electrical Engineering and Computer Sciences from the University of California, Berkeley, in 1989, 1990, and 1994 respectively. Since September 1994, he has been the Analog Devices career development assistant professor of Electrical Engineering at the Massachusetts Institute of Technology, Cambridge. He received the NSF Career Development award in 1995, the IBM Faculty Development award in 1995 and the National Semiconductor Faculty Development award in 1996. He received the IEEE Communications Society 1993 Best Tutorial Paper Award for the IEEE Communications Magazine paper titled, "A Portable Multimedia Terminal". His research interests include the ultra low power implementation of custom and programmable digital signal processors, wireless sensors and multimedia devices, emerging technologies, and CAD tools for VLSI. He is a co-author of the book titled "Low Power Digital CMOS Design" by Kluwer Academic Publishers.



Robert W. Brodersen received Bachelor of Science degrees in Electrical Engineering and in Mathematics from California State Polytechnic University, Pomona, California in 1966. In 1968 he received the Engineers and M.S. degrees from the Massachusetts Institute of Technology, (MIT) Cambridge, and he received a Ph.D. in Engineering from MIT in 1972.

From 1972–1976, Brodersen was with the Technical Staff, Central Research Laboratory at Texas Instruments, Inc., Dallas. He joined the Electrical Engineering and Computer Science faculty at the University of California at Berkeley in 1976, where he is currently a professor. In addition to teaching, Professor Brodersen is involved in research inclusive of new applications of integrated circuits, focused in the areas of low power design and wireless communications.

He has won conference best paper awards at Eascon (1973), International Solid State Circuits Conference (1975) and the European Solid State Circuits Conferences (1978).

Professor Brodersen received the W.G. Baker award for the outstanding paper in the IEEE Journals and Transactions (1979), Best Paper Award in the Transactions on CAD (1985) and the Best Tutorial paper of the IEEE Communications Society (1992).

In 1978 Professor Brodersen was named the outstanding engineering alumnus of California State Polytechnic University. He became a Fellow of the IEEE 1982. He was co-recipient of the IEEE Morris Libermann award for "Outstanding Contributions to an Emerging Technology," in 1983. And he received Technical Achievement Awards from the IEEE Circuits and Systems Society in 1986 and in 1991 from the IEEE Signal Processing Society.

Professor Brodersen was elected a member of the National Academy of Engineering in 1988. In September of 1995, he was appointed the first holder of the John R. Whinnery Chair in Electrical Engineering at University of California, Berkeley.