

Baseband Filter and $\Sigma\Delta$ Converter for Wideband RF receiver

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ABSTRACT

This paper describes a fully-differential anti-alias filter (AAF) and analog-to-digital converter (ADC) for baseband processing of a wideband RF signal. The AAF is a third order elliptic low-pass filter. The ADC is a 2-2 cascade sigma-delta architecture with a single-bit quantizer in the first stage and a 13-level quantizer in the second stage. The system converts a 2.5 MHz input signal (5 Ms/s Nyquist rate) at an oversampling ratio (OSR) of 16, and it achieves a peak SNDR of 72.3 dB.

1.0 SYSTEM SPECIFICATIONS

The RF specifications used in this project are a combination of the specifications extracted from the Infopad-2 system, systems using the emerging UMTS standard, and system using the existing GSM standard. A simplified model of the RF channel characteristics is shown in Figure 1. In this model, it is assumed that there is one near-band interferer at a 1 MHz away from the signal and one far-band interferer residing at the sampling frequency. With this model, the resultant baseband performance requirements can be extracted. These calculations can be found in [1], and they are summarized in Table 1; in particular, the dynamic range requirement is 71.4 dB at a Nyquist conversion rate of 5 Ms/s.

1.1 Baseband Architecture Selection

In [1], it was shown that due to the presence of a strong near-band interferer, the anti-aliasing filter requirements became impractical for OSR's below 10. Thus, two possible architectures were either an oversampled switched-capacitor filter (SCF) followed by a Nyquist-rate converter, or an oversampled sigma-delta modulator ($\Sigma\Delta$) followed by a digital decimation filter. It was shown in [1] that for

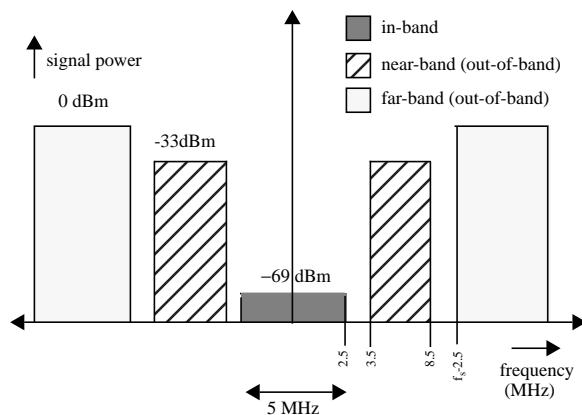


Figure 1. In-Band and Out-of-Band Signal Levels.

OSR's in the range of above 10, the required order of the SCF was equal to or greater than the required order of a $\Sigma\Delta$ for the given dynamic range requirements. Furthermore, thermal noise in a SCF is directly proportional to the number of stages, whereas thermal noise in later stages of a $\Sigma\Delta$ is suppressed by its noise-shaping characteristic. Thus, power dissipation in a thermal-noise limited SCF of a given order will be higher than that in a comparable $\Sigma\Delta$. For these reasons, a $\Sigma\Delta$ architecture was chosen.

2.0 ANTI-ALIAS FILTER

2.0.1 Anti-alias filter specifications

As will be explained in Section 3.0, the OSR selected to be 16. Given this, the AAF specifications are derived and summarized below. $f_{\text{pass}} = 2.5$ MHz, $f_{\text{stop}} = 77.5$ MHz; $R_{\text{pass}} < 1$ dB, $R_{\text{stop}} > -76$ dB; In-band $\Delta\text{grd} < 40$ ns; $V_{\text{fs}} = 1.8$ V, $\text{DR} > 76$ dB, and so, In-band $V_{\text{noise}}(\text{rms}) < 57.03$ μV . Detailed calculation is attached in Appendix B.

2.0.2 Anti-alias filter architecture

Based on the specs given above, MATLAB was used to decide the filter type and order. As shown in Table 2, we calculated the filter order needed for different types of filters corresponding to different amount passband ripple and process variation. Three conclusions can be drawn from this table:

1. Frequency tuning is not necessary. Up to 30% band-edge shift at 0.1 dB passband ripple, a 3-rd or 4-th order meet the specs.
2. Designing for $R_p = 0.1$ dB typically won't increase filter order beyond that required for $R_p = 1$ dB.
3. Designing for $R_p = 0.1$ dB, 30% bandedge shift, elliptic filter is one order than other types, which means some hardware saving and power reduction.

So a 3-rd order elliptic filter with $R_p = 0.1$ dB was used to accommodate further performance degradation caused by various nonidealities. Compared with Butterworth and Chebyshev filters, the elliptic filter has a slightly higher group delay spread, but it turns out with the large transition width and low order, phase nonlinearity of this 3-rd order elliptic filter still resides inside spec.

An RC structure is chosen vs. MOSFET-C and Gm-C structure is because this is a simple AAF. As will be shown in Section 2.0.3, since we can tolerate the circuit sensitivity

to process variation, and since the filter is low order, a ladder is not needed. It should be noted that the oversampling nature of the converter greatly alleviates the difficulty of AAF design.

2.0.3 Anti-alias filter circuit implementation and simulation results

A circuit diagram of the equivalent single-ended 3rd-order RC filter is shown in Figure 9. A first order stage is followed by a biquad. Pole-zero cancellation was done to reduce the opamp unity-gain bandwidth requirement. In the real differential circuit implementation, all the capacitor value halves, and all the resistor value doubles. So, for the differential circuit implementation, $C_{min}=25\text{fF}$, $C_{max}=3.85\text{PF}$, $\text{spread}=154$. The negative resistor value can be achieved by proper connection of the positive and negative branches. All the opamp gain are set to 1000, unity-gain bandwidth is 15MHz.

First, circuit parameters with ideal opamp are calculated in matlab to achieve the ideal transfer function. In hspice, the nominal, slow and fast case with process variation $\Delta R/R=\pm 20\%$, $\Delta C/C=\pm 10\%$ were checked to make sure circuit performance is within specification. Resistor and capacitor values were scaled to adjust each opamp output gain referred to input is less or equal to 1. Component values were adjusted to get the minimum capacitor value spread and minimum total capacitor value while remaining within the total noise budget. After scaling, the filter with ideal opamp can achieve $R_p=0.1\text{ dB}$, $R_{stop}=-81\text{dB}$, $\Delta\text{grd}=34\text{ns}$, $V_{noise(rms)}=56\mu\text{V}$. All are worst-case measurement and are within specification.

Before considering opamp nonideality, effect from component mismatch is investigated by Monte-Carlo analysis in hspice. Shown in Figure 10, the dashed lines represent the case of ideal opamp. Up to 5% mismatch, specifications are met. Component mismatch affects passband ripple more severely than global process variation but given 0.5% mismatch tolerance in our project, component mismatch is not an issue at all. By contrast, group delay spread, noise are sensitive to global process variation, so worst-case check is important.

Circuit performance degradation caused by finite opamp gain, finite unity-gain bandwidth is studied too. Figure 11 shows finite gain effect. Both passband ripple and group delay spread are not affected until gain is lower than about 1000. Stopband attenuation is not affected too much. So, 1000 is chosen as the opamp gain in our design though with gain lower than that, eg, 100, the circuit is still working within specifications.

Figure 12 shows how the unity-gain bandwidth affect circuit behavior. On the left, the plot shows without pole-zero cancellation, giving some safety margin for component mismatch, 30MHz is the required unity-gain frequency.

With pole-zero cancellation, 10MHz is the required unity-gain frequency. On the right, it shows finite unity-gain bandwidth helps reduce passband groupdelay spread. And it is not shown here but true that finite unity-gain bandwidth helps attenuation at stopband edge too. 15 MHz is chosen as the unity-gain frequency for our design.

Overall, a 3rd-order elliptic RC filter was designed for a 3.3 μm process. Opamp gain requirement is 1000. Opamp unity-gain frequency requirement is 15MHz. Overall performance achieved is summarized below,

$$R_p < 0.6\text{ dB}, R_{stop} < -76\text{ dB}, \Delta\text{grd} < 24\text{ ns}$$

$$V_{noise(rms)} = 55\mu\text{V}$$

This result also pass the Monte-Carlo check, shown in Figure 10. The Hspice input deck is attached.

3.0 $\Sigma\Delta$ MODULATOR

Due to the high bandwidth of the signal to be acquired, the modulator was designed to allow suitable performance at a low OSR. This design choice requires the use of high-order, multi-bit $\Sigma\Delta$ structures. A more complex, low-OSR structure will also tend to be a lower power solution, as the power of the modulator increases much more dramatically with increased OSR than with increased order.

$$SQDR = \frac{3}{2} \left(\frac{2L+1}{\pi} \right) (Q-1)^2 M^{2L+1} \quad (1)$$

Equation (1) shows ideal peak SQDR¹, where L is the modulator order, Q is the number of quantization levels, and M is the OSR. Table 3 lists necessary OSR's needed to meet a given peak SQDR requirement for given a order and number of quantization bits. As CDMA communications systems are robust to discrete tones (i.e. fixed pattern noise), it was deemed that the total noise power from quantization and distortion should be about 6 dB below the thermal noise floor. Therefore, the system was designed for a peak SQDR of 78 dB.

From Table 3, we can extract the necessary modulator order and quantizer resolution to achieve our dynamic range at reasonable OSR. It was determined that a fourth-order loop with 3-4 bits in the quantizer was sufficient to achieve our design specification while providing enough margin for deviation from ideal calculations. In particular, Table 3 does not take into account two major sources of SQDR loss in high-order structures, namely:

1. Inter-stage gain coefficients below unity in cascaded structures.

1. In this paper, SQDR refers to signal-to-quantization-and-distortion ratio, and it accounts for all non-idealities *except* thermal noise.

2. SQDR loss due to stability problems in single-loop structures.

Due to these sources of SQDR loss in high-order $\Sigma\Delta$ modulators, a margin of 15 dB over the ideal SQDR presented in Table 3 was included in our calculations.

3.0.1 Single-ended vs. Differential structure

A differential switched-capacitor structure, as depicted in Figure 7 (b), was chosen for circuit implementation. As shown in Appendix A, this circuit implementation will have roughly the same power consumption and dynamic range as the single-ended structure shown in Figure 7 (a). The differential structure, however, will be more robust to circuit non-idealities such as even-order harmonic distortion and power supply fluctuation. Therefore, a differential circuit structure will be used. For the sake of simplified analysis, all analysis in the paper will be done on the equivalent single-ended structure unless otherwise noted.

3.0.2 Full-Delay Integrators vs. Resonators

Our design uses a cascade of full-delaying integrators with distributed feedback. Thus, our design places all the noise transfer function (NTF) zeros at DC. $\Sigma\Delta$ modulators can achieve more aggressive noise-shaping by optimally placing the NTF zeros across the signal band [2]. In order to accomplish this, switched-capacitor resonator structures with some form of local feedback must be used. True resonators require non-delaying integrators in the feed-forward path, and thus double op-amp settling. Due to the already high-speed operation of the modulator in question, this approach was avoided. Pseudo-resonators can also be constructed using full-delay integrators, yet it was found empirically that the coefficient spread (and thus capacitor spread) of such an approach was too large to be practical.

3.0.3 Single-loop vs. cascade

Our design uses a 2-2 cascade $\Sigma\Delta$ architecture. As is shown in [2], high-order single-loop modulators with single-bit quantizers perform far below ideal SQDR predictions due to potential instability. At OSR's below 20, increasing a single-bit loop beyond second-order results in a loss in SQDR [2]. Hence, single-bit single-loop architectures with order above two were eliminated from consideration.

With a sufficient number of quantization levels, however, the performance of single-loop architectures is supposed to approach the ideal SQDR limit [3]. Performance degradation due to DAC non-linearity can be suppressed using dynamic-element matching techniques, as in [4]. Attempts were made to stabilize a fourth-order, multi-bit single-loop $\Sigma\Delta$ modulator for this project, but no architecture could be designed that didn't overly suffer from peak SQDR loss due to instability problems.

A 2-2 cascade is attractive due its increased stability and fourth-order noise-shaping characteristic. There are two primary drawbacks to a cascaded architecture, however. First, an interstage gain coefficient of less than unity is typically needed, thus requiring a gain of greater than unity in the recombination network. This digital gain will amplify the noise, thus directly reducing SQDR. This was compensated for by adding the 15 dB design margin described above. Also, a cascade architecture is more sensitive to component variation as the deterministic digital gain must precisely match mismatch-determined analog interstage gain. Mismatch between the analog and digital gain will result in leakage of an error term shaped only by the first stage. Therefore, a first-stage of high-order is desirable. As mentioned previously, at low OSR there is no advantage to increasing the order of a single-loop beyond 2; hence our choice of a second-order first stage. Calculations described in section 3.2.2 determined that our architecture would be robust to the mismatch under the given process variation parameters.

3.0.4 Single-bit vs. multi-bit quantization

The first stage of the cascade has a single-bit quantizer for ease of implementation and DAC non-linearity constraints. The second stage has a 13-level quantizer and DAC (12 decision levels). As demonstrated in Section 3.2.4, the non-linearity error introduced by the quantizer is suppressed by fourth-order shaping, and the error introduced by the DAC is suppressed by second-order shaping. The errors introduced by these two non-idealities were small enough to allow the use of 13-level quantization with minimal loss in SQDR from the ideal case.

3.1 Modulator Coefficients

Figure 13 shows the single-ended equivalent structure of the 2-2 $\Sigma\Delta$ modulator. The coefficients were designed to allow aggressive noise-shaping over a maximal stable input range. An initial set of coefficient values were taken from the first two stages of the 2-2-2 cascade described in [5]. Due to the addition of the 13-level quantizer in the second stage, the coefficients in the second stage were adjusted to sufficiently exercise all the levels of the ADC. This process was iterated several times to ensure maximal input stable range. Table 4 lists final values of the coefficients. The input stable range was determined by a million-step DC input test. Figure 2 shows the maximum integrator output vs. input DC level. It can be seen that all integrator outputs remain below fullscale for inputs less than 80% fullscale. Thus, the maximum input signal is set at -2 dBFS in order to prevent integrator clipping.

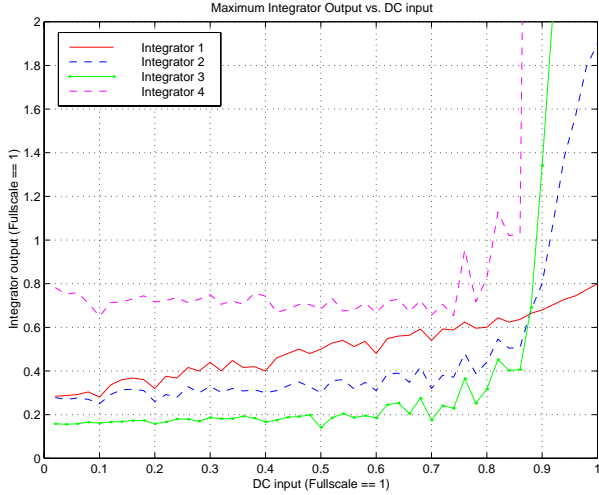


Figure 2: Maximum integrator output vs. DC input

Once the coefficients are chosen, the necessary digital recombination circuitry can be determined:

$$Y(z) = H_1(z)Y_1(z) + H_2(z)Y_2(z) \quad (2)$$

$$H_1(z) = \lambda z^{-2} - 2(\lambda - 1)z^{-3} + (\lambda - 1)z^{-4} \quad (3)$$

$$H_2(z) = \frac{1}{g_d}(1 - z^{-1})^2 \quad (4)$$

$$g_d = \frac{a_{f1}a_{i2}a_{u3}}{a_{f3}} = 0.25 \quad (5)$$

$$\lambda = \frac{a_{i3}}{a_{f1}a_{i2}a_{u3}} = 2 \quad (6)$$

where g_d is the digital approximation of the interstage gain coefficient. For the sake of simple digital circuits, g_d is constrained to be a power of two.

3.2 $\Sigma\Delta$ performance analysis

Figure 14 shows a linear model of the $\Sigma\Delta$ with the quantizers and DAC's replaced with white noise sources. While the error introduced by these components is not white, previous analysis has shown that the white noise approximation is reasonable for analysis[6].

3.2.1 Second-stage quantization noise

Assuming perfect digital recombination, the spectrum of the output signal is given by equation (7):

$$Y(z) = z^{-4}X(z) + \frac{1}{g_d}(1 - z^{-1})^4 E_2(z) \quad (7)$$

The error term from the first quantizer is ideally cancelled, and the error term from the second quantizer undergoes fourth-order shaping and amplification by $1/g_d = 4$. Hence, the output noise is amplified by 12 dB above the ideal fourth-order case, and this 12 dB is directly subtracted from ideal peak SQDR. A 13-level quantizer was chosen to make this error term -88.5 dBFS, and hence small when compared to the desired peak SQDR of 78 dB.

3.2.2 Analog/Digital Mismatch

As shown in equation (5), g_d is a digital gain coefficient representing the product of 4 independent capacitor ratios. These four capacitor ratios comprise 7 independent capacitors (the third integrating capacitor defines both a_{u3} and a_{f3} .) Therefore, gain mismatch, δg , should be $\sqrt{7}$ times the capacitor mismatch, δc . ($\delta g = \delta c \sqrt{7} = 1.3\%$)

With a mismatch of δg , the spectrum of the output signal becomes:

$$Y = z^{-4}X + (\delta g)z^{-2}(1 - z^{-1})^2 E_1 + \frac{1}{g_d}(1 - z^{-1})^4 E_2 \quad (8)$$

Analog/digital mismatch prevents perfect cancellation of the first-stage error noise, and thus allows leakage of a second-order shaped error term. At 1.3% mismatch, the power of the error leakage term is -83 dBFS, and analytical calculations predict that 79 dB peak SQDR can be attained with up to 2% mismatch. This error leakage term will be the performance-limiting factor for this $\Sigma\Delta$ modulator at higher OSR's. Thus, with $\text{OSR} \gg 16$, SQDR will only improve at roughly 15 dB/octave.

Figure 3 shows theoretical and simulated peak SQDR, modelling the two error sources shown in equation (8). Correlation between simulated points and analytical predictions is very good, suggesting that the white noise approximation is valid in this situation.

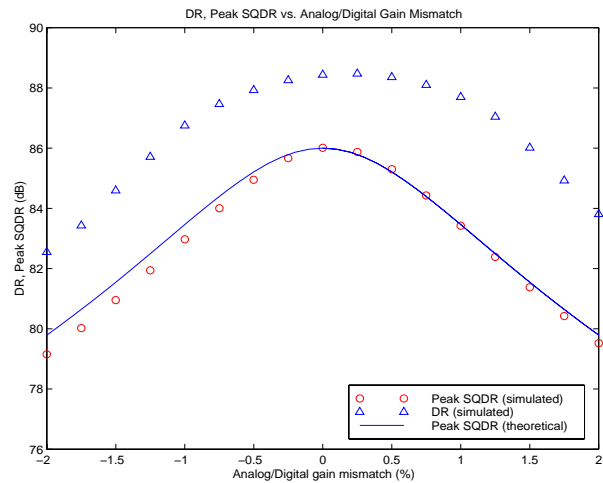


Figure 3: Peak SQDR vs. A/D gain mismatch

3.2.3 Finite DC Amplifier Gain

Ideal integrators have infinite gain at DC. In actual switched capacitor integrators, finite DC op-amp gain will move the integrator pole inside the unit circle, resulting in a “leaky” integrator. An expression for the new integrator transfer function is:

$$I_{act}(z) = \frac{a_i}{1 - (1 - \varepsilon)z^{-1}} \quad (9)$$

$$\varepsilon = 1 - \frac{1}{1 + \frac{a_i}{A_{vo}}} \cong \frac{a_i}{A_{vo}} \quad (10)$$

where a_i is the integrator gain as set by the capacitor ratio, C_s / C_i , and A_{vo} is the opamp DC gain.

With this new integrator transfer function, the spectrum of the output signal can be calculated (ignoring g_d mismatch):

$$Y = z^{-4}X + [z^{-4}(\varepsilon_1\varepsilon_2) + z^{-3}(1 - z^{-1})(\varepsilon_1 + \varepsilon_2)]E_1 + \frac{1}{g_d}(1 - z^{-1})^4 E_2 \quad (11)$$

where $\varepsilon_1, \varepsilon_2$ are the leakage terms for the first and second integrators. The leakage from the third and fourth integrators appear only in higher-shaped terms and their effects will be negligible in comparison to $\varepsilon_1, \varepsilon_2$. The middle term of equation (11) shows that leaky integrators will cause leakage of both unshaped and first-order shaped quantization error. The unshaped error is proportional to the product of the first two leakage factors, and will be negligible for reasonable gains. The first-order-shaped error is proportional to the sum of the first two leakage constants. Therefore, the op-amps’ DC gain must be high enough to make this term negligible. From equation (11), it can be calculated that DC gains of 700 result in leakage of an error term which is -91 dBFS, and hence negligible. Figure 4 shows a plot of peak SQDR vs. op-amp DC gain (with 2% a/d gain mismatch). As can be seen on this plot, DC gains above 600 results in a loss of less than 1 dB. For very low gains, simulated results are much lower than predicted results. This is because low DC gains also affect the numerator of the integrator’s transfer function, thus exacerbating analog/digital gain mismatch.

For the purposes of our design, an amplifier gain of 700 was chosen. This should minimally affect peak SQDR performance. With the selection of an actual silicon process, however, caution should be made to make sure that the op-amp is sufficiently linear over its full-scale operating region. For this reason, op-amps with higher DC gain may be needed.

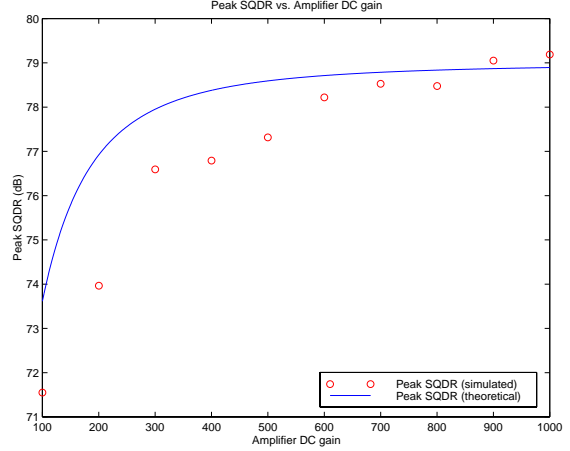


Figure 4: Peak SQDR vs. op-amp DC gain

3.2.4 Quantizer and DAC Non-Linearity

The 13-level quantizer is a flash architecture, consisting of 12 fully differential comparators referenced to a resistor string as shown in Figure 15(a). In actuality, this comparator will suffer from non-linearity errors due to resistor mismatch, op-amp offset, hysteresis, and other such phenomenon. All of these non-idealities can be represented as an additional error term added at the quantizer. Thus this non-linearity error is shaped by fourth-order differentiation just as the quantization noise from this quantizer is shaped. Therefore, provided that the quantizer is monotonic, (i.e. its non-linearity error power is less than its quantization error power), the quantizer can be treated as an ideal component.

The DAC is comprised of a 13-level differential resistor string as shown in Figure 15(b), similar to that in [7]. Due to resistor mismatch, the DAC will also add an error term to the signal output. As the error is added directly into the signal path at the input to the second stage, the DAC error term does not undergo any shaping in the modulator. The error term is shaped by second-order differentiation in the recombination filter; hence the output signal looks like:

$$Y = z^{-4}X + \dots + \frac{1}{g_d}(1 - z^{-1})^2 E_{DAC} \quad (12)$$

where E_{DAC} is the white noise approximation for the error inserted due to DAC non-linearity. For 0.5% mismatch, E_{DAC} was calculated to be roughly -46.5 dBFS (see Appendix C for calculation of E_{DAC} .) The second-order differentiation of E_{DAC} suppresses its power by another 49 dB. Hence, the error term for E_{DAC} at 0.5% component mismatch should be roughly -95.4 dBFS, a negligible term when compared to other noise sources.

Random resistor mismatches were generated, and it was found empirically that the modulator could tolerate a mismatch σ of up to 1.5% without the 6σ -SQDR dropping below 80 dB (see Figure 5). Theoretical results match well with simulated results, as explained in Appendix C.

It is worth noting that the choice of a differential architecture greatly assists in suppressing non-linearities in the DAC by removing second-order harmonics. Viewed in another manner, it can be observed that the DAC output has no error at positive and negative full-scale *and at zero output*. The fact that the DAC error is “pinned” to zero at three points on its transfer function limits the maximum INL deviation that the DAC can reach. Thus, a differential DAC will be inherently more linear than a single-ended DAC.

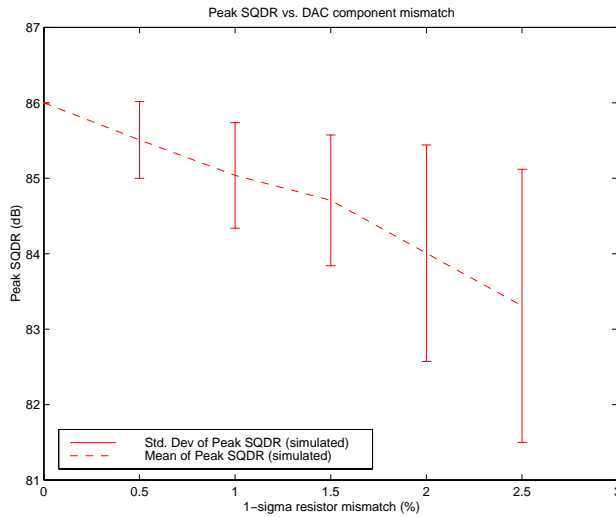


Figure 5: Peak SQDR vs. DAC component mismatch (100 simulations at each mismatch point)

The values of the resistor strings can be calculated for appropriate settling of the ADC and DAC, and these calculations are shown in Appendix D. Due to the small capacitances used, the total resistance of the resistor strings for the DAC and ADC can be as big as 11.1 k Ω and 20 k Ω , respectively (unit R sized at 925 Ω , 1.6 k Ω). Thus, less than 0.5 mW in total will be dissipated by these resistor strings.

3.2.5 Slew-rate limiting and linear settling

It has been shown that every integrator in a $\Sigma\Delta$ modulators does not need to settle to the full precision of the converter [8]. In particular, errors introduced by incomplete settling in integrators further down the modulator chain are shaped by the integrators preceding it when referred to the input. MIDAS simulations were used to determine necessary settling requirements. Figure 16(a)-(d) show contours of constant peak SQDR for given settling parameters in each integrator. As can be seen in these figures, the settling requirements are relaxed in integrators further down the chain.

The desired performance was 78 dB peak SQDR. Assuming a clock speed of 80 MHz, and 2.5ns overhead for clock non-overlap (i.e. 5ns of settling), the required settling performance for each integrator can be determined (see Table 5). Note that the first integrator has two acceptable design points: one which is slew-rate dominated and one that is settling dominated. With the selection of the actual silicon process, it would remain to be determined as to which design point results in optimal power dissipation. Some further amount of over-design will be required due to the fact that MIDAS simulations assume the opamp has only a single pole. The settling requirements are relaxed further down the $\Sigma\Delta$ pipeline, with the exception of the fourth integrator slewing requirement. It is inferred that this integrator needs a higher slew rate than otherwise expected in order to sufficiently exercise all DAC levels.

3.2.6 Thermal noise and capacitor sizing

Sampling capacitors must be sized to allow the required 71.4 dB of dynamic range. It is worth noting that the noise-shaping characteristic of $\Sigma\Delta$ modulators shapes the thermal noise from amplifiers further down the pipeline; thus, the dominant source of thermal noise is from the first sampling capacitor, and sampling capacitors from later integrators can be reduced in size for power optimization. The total thermal noise power of the 2-2 cascade can be expressed as: [5]

$$S_{N, total} = \frac{S_{N1}}{M} + \frac{\pi^2 S_{N2}}{a_{i1}^2 M^3} + \frac{\pi^4 S_{N3}}{a_{i1}^2 a_{i2}^2 M^5} + \frac{\pi^6 S_{N4}}{a_{i1}^2 a_{i2}^2 a_{i3}^2 M^7} \quad (13)$$

$$S_{Ni} = \gamma \frac{kT}{C_{si}}$$

where γ is a multiplicative factor to account for amplifier noise factor and $1/f$ noise. Since this is a wideband application, it was assumed $1/f$ noise would not be totally dominant, and a γ factor of 3 was assumed. Table 5 lists the total sampling capacitance needed for each integrator. It was assumed that a minimum-sized capacitor of 25 fF (25 μm by 25 μm metal caps at 0.4 fF/ μm^2) were available. The thermal noise from the third and fourth integrator is suppressed to such a degree that its capacitor size is dictated by this process limitation (which makes the sampling capacitance larger than desired due to coefficient spread). Assuming a V_{FS} of 1.8V and a maximum input sinusoid of

-2 dBFS, peak SNDR is predicted to be 72.1 dB. A simplified, single-ended equivalent diagram of the modulator is shown in Figure 22.

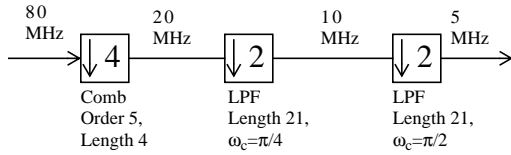


Figure 6: Decimation Filter structure

3.3 Decimation Filter

A diagram of the decimation filter is shown Figure 6. It consists of a order 5, length 4 decimate-by-four comb filter, followed by two decimate-by-two, length 21 low pass digital filters. This 3-stage design is necessary to sufficiently suppress the near-band blocker; if a two-stage design were used (with a decimate-by-8 comb), the near-band blocker would alias into the signal band without sufficient suppression. The filters' frequency responses are shown in Figure 17, and their coefficients are included in the attached MIDAS deck.

4.0 SIMULATION RESULTS

Simulink was used to verify first-order calculations for the $\Sigma\Delta$ modulator, and MIDAS was used to extensively simulate the modulator and its various non-idealities. Matlab was used to generate random mismatch parameters. All relevant files and flowcharts are attached.

Figure 18 shows a MIDAS simulation of SQDR vs. input amplitude range. In this figure, all non-idealities were simulated, except thermal noise. The design point was a peak SQDR of 78 dB (i.e. quantization-and-distortion noise power 6 dB below the thermal noise floor). Simulations verified a peak SQDR of 79.4 dB.

Figure 19 shows a MIDAS simulation of SNDR vs. input amplitude range. In this simulation, all non-idealities discussed were included; hence the design target was 71.4 dB dynamic range. Simulations showed a DR of 72.2 dB and a peak SNDR of 72.3 dB. Figure 20 and Figure 21 shows the FFT of the output signal (input at -2 dBFS) after and before decimation. Figure 21 shows the typical noise-shaping characteristic, and one can observe in Figure 20 that there are no strong idle tones present.

5.0 REFERENCES

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APPENDIX A SINGLE-ENDED VS. DIFFERENTIAL CIRCUITS

This appendix is used to show the power and dynamic range equivalencies between similarly structured single-ended and differential switched-capacitor circuits.

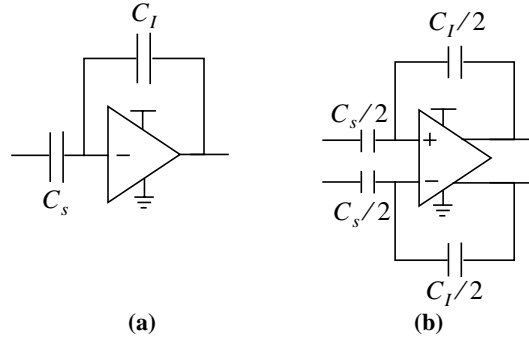


Figure 7: (a) Single-ended structure
(b) Equivalent differential structure

First, assume a single-ended circuit structure, as shown in Figure 7 (a). Here the gain of the circuit is unity, but the following argument is applicable for non-unity gain. The peak-to-peak output swing of the amplifier (assuming common-source output stage) is:

$$V_{o,pp} = V_{dd} - 2V_{dsat} \quad (14)$$

Hence, the peak signal power is:

$$P_{sig} = \frac{V_{o,pp}^2}{8} \quad (15)$$

And the thermal noise, from equation (13) is:

$$S_N = \gamma \left(\frac{2kT}{C_s} \right) \quad (16)$$

Therefore, the dynamic range for a single-ended structure can be expressed as:

$$DR = \frac{P_{sig}}{S_N} = \frac{(V_{dd} - 2V_{dsat})^2 C_s}{16\gamma(kT)} \quad (17)$$

In the case of the differential structure shown in Figure 7 (b), the following equations hold:

$$\begin{aligned} V_{o,pp} &= 2(V_{dd} - 2V_{dsat}) \\ S_N &= 2\gamma \left(\frac{2kT}{C_s/2} \right) = 4\gamma \left(\frac{2kT}{C_s} \right) \end{aligned} \quad (18)$$

The output swing is doubled, due to the differential nature of the circuit. The thermal noise is quadrupled: a factor of 2 comes from the fact that the individual capacitor sizes are halved; the other factor of two is due to the differential nature of the circuit, and hence double the number of noise sources.

When these new values are plugged back into equation (17), it is found that the single-ended and differential structures shown in Figure 7 have the same dynamic range.

These two structures also have the same power consumption to first-order. This can be seen as the differential structure has twice as many current legs (due to its differential nature), but each current leg must run only half as much current due to the fact that it drives a half-sized capacitance.

As the two structures are similar in terms of dynamic range and power, the differential structure was chosen due to its robustness to power supply variation and even-order distortion. Equivalent single-ended structures (via the transformation described above) were used in all analysis for the sake of simplicity.

APPENDIX B ANTI-ALIAS FILTER SPECIFICATIONS CALCULATION

As explained in Section 3.0, an oversampling ratio of 16 was selected. Given signal bandwidth 2.5MHz, ADC sampling frequency is 80MHz. So, AAF passband edge $f_p = 2.5$ MHz, stopband edge $f_{stop} = f_s - 2.5\text{MHz} = 77.5$ MHz.

Passband ripple (1 dB) and passband group delay spread (40 ns, corresponding to 10% period @ 2.5 MHz) were chosen following typical commercial AAF examples for the similar communication systems.[9]

The required carrier to noise ratio for the system is 15 dB Table 1. The far-end interferer is 69 dB stronger than the desired signal. Noting RF receiver before the AAF has 13 dB attenuation at 80 MHz from the carrier [1], given 5dB safety margin, the stopband attenuation $R_{stop} = 15+69-13+5 = 76$ dB. And for the same argument, required DR is 76 dB.

In-band noise requirement is calculated below for DR= 76 dB for the equivalent single-ended circuit. As discussed in section 3.1, maximum input signal for a stable SD modulator following the AAF is 0.8 full scale range. So, maximum AAF output V_{p-p} is $0.8 \cdot V_{fs}$.

$$P_{signal} = \frac{(0.8V_{fs})^2}{8} = \frac{(0.8 \times 1.8V)^2}{8} = 0.2592V^2 \quad (19)$$

and $DR = 10 \cdot \log_{10}(P_{signal} / P_{noise})$, for DR= 76 dB, $P_{noise} = 6.506 \text{ nV}^2$ (from -2.5MHz to 2.5MHz), hence,

$$V_{noise}(rms) = \sqrt{(P_{noise}/2)} = 57.03\mu V \quad (20)$$

for frequency from 0 to 2.5MHz.

APPENDIX C WHITE-NOISE ESTIMATE OF DAC NON-LINEARITY ERROR

This appendix is used to derive an approximation of the power of E_{DAC} shown in Figure 14 based on the differential resistor-string DAC (RDAC) architecture of Figure 15(b).

It is important to note that a differential N-level RDAC is inherently more linear than a single-ended N-level RDAC. This characteristic can be explained as follows: assuming the digital input spans plus/minus fullscale, both DAC structures have a perfect output (i.e. no error) at plus or minus full-scale digital input. The single-ended RDAC will have its worst case error at midscale (i.e. digital zero) input. The differential output at midscale, however, *will be identically zero* (see Figure 15(b)); hence it will have no error at midscale. This will in effect clamp the maximum error value and result is a more linear RDAC structure. Viewed another way, a differential RDAC is free from even-order non-linearity.

A differential RDAC structure has odd symmetry; hence the non-linearity of half of the structure (digital input from zero to fullscale,) can be analyzed and attributed to negative digital inputs.

In determining the total power of E_{DAC} , it was assumed that all the levels of the DAC were exercised with equal probability ($P_i = 1/13$). This assumption was deemed valid due because the input to the second-stage was the error output of the first stage (assumed white), and the DAC would be forced by feedback to track the input.

Under these assumptions, E_{DAC} was calculated as follows:

$$\begin{aligned}
Power(E_{DAC}) &\cong E[\sigma_{DAC}^2] \\
&= \frac{1}{13} \sum_{n=-6}^6 [\sigma_{DAC}(n)^2] \\
&= \sigma_{DAC}(0)^2 + \frac{2}{13} \sum_{n=1}^6 [\sigma_{DAC}(n)^2] \\
&= 0 + \frac{2}{13} \sum_{n=1}^6 [\sigma_{DAC}(n)^2] \\
&= \frac{2}{13} \sum_{n=1}^6 \sigma_R^2 \left(1 - \frac{n}{6}\right)^2 \\
&= \frac{35}{39} \sigma_R^2
\end{aligned} \tag{21}$$

where $\sigma_{DAC}(n)$ is the standard deviation of the analog error for a digital input n .

For a resistor mismatch (σ_R) of 0.5%, the power of E_{DAC} is predicted to be roughly -46.5 dBFS. Second-order differentiation in the digital recombination filter suppresses this noise by an additional 49 dB; hence, at 0.5% component mismatch, we expect the in-band power of E_{DAC} to be roughly -95.5 dBFS.

From Figure 5, we can see that average peak SQDR drops from 86 dB to 85.5 dB with the addition of 0.5% DAC component mismatch. The 0.5 dB drop corresponds to an additional noise term (DAC noise) that is 9 dB below the pre-existing noise term (second-stage quantization noise). Hence, simulations show that the expected power of the DAC noise is -86 dBFS - 9 dB, or -95 dBFS. As demonstrated in the previous paragraph, calculations predict the DAC noise power to be -95.5 dBFS.

APPENDIX D DAC/ADC RESISTOR STRING CALCULATION

A simplified model of the DAC is shown in Figure 8a. Here R_T is the total value of the resistor string, R_{sw} is the switch resistance, and the 200 fF capacitor is the total feedback capacitance seen (from the third and fourth integrator). C_{gd} and C_{db} will be on the order of a few fF for reasonably small transistors, and hence will be ignored in this analysis. (In other words, signal coupling via overlap capacitance from the clock signal will be negligible.)

Therefore, the settling time constant for the DAC will be roughly:

$$\tau = \left(\frac{R_T}{4} + R_{sw} \right) 200 \text{ fF} \tag{22}$$

A conservative design choice is to allow the DAC to settle to the full resolution of the converter plus some safety margin (i.e. 80 dB). This implies roughly 9.2 τ 's of settling are required in 5 ns ($\tau = 555$ ps). Using the parameters from the 0.35 μm process given, choosing the W/L of the switch to be 10 ($3.5\mu\text{m} / 0.35 \mu\text{m}$) will allow sufficient settling if $RT/4$ is less than 2.78 k Ω . This implies a total string resistance of 11.1k Ω or a unit resistance of 925 Ω .

A simplified model of a single comparator of the ADC is shown in Figure 8b. Here signal coupling from the output back to the reference input must be considered. In this case, the switching of a comparator output will capacitively feedthrough to the voltage reference node; if this feedthrough effect is not sufficiently settled out, the quantizer may produce an error at its output. Again, allowing for 80 dB of settling in 5ns, a similar calculation can be made. Note that this is a *very* conservative design choice, as the quantizer error will be shaped by fourth-order differentiation. Due to the very small capacitances of the comparator input (roughly 20 fF for a 1.75 μm by 0.35 μm transistor), the ADC string will settle easily with a string resistance as large as 20 k Ω .

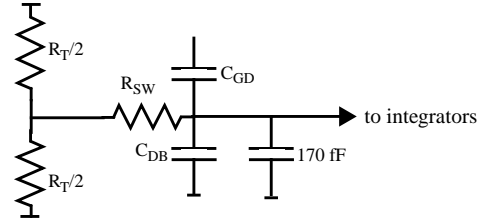


Figure 8a: Simplified DAC settling model

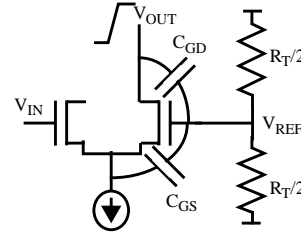


Figure 8b: Simplified comparator model

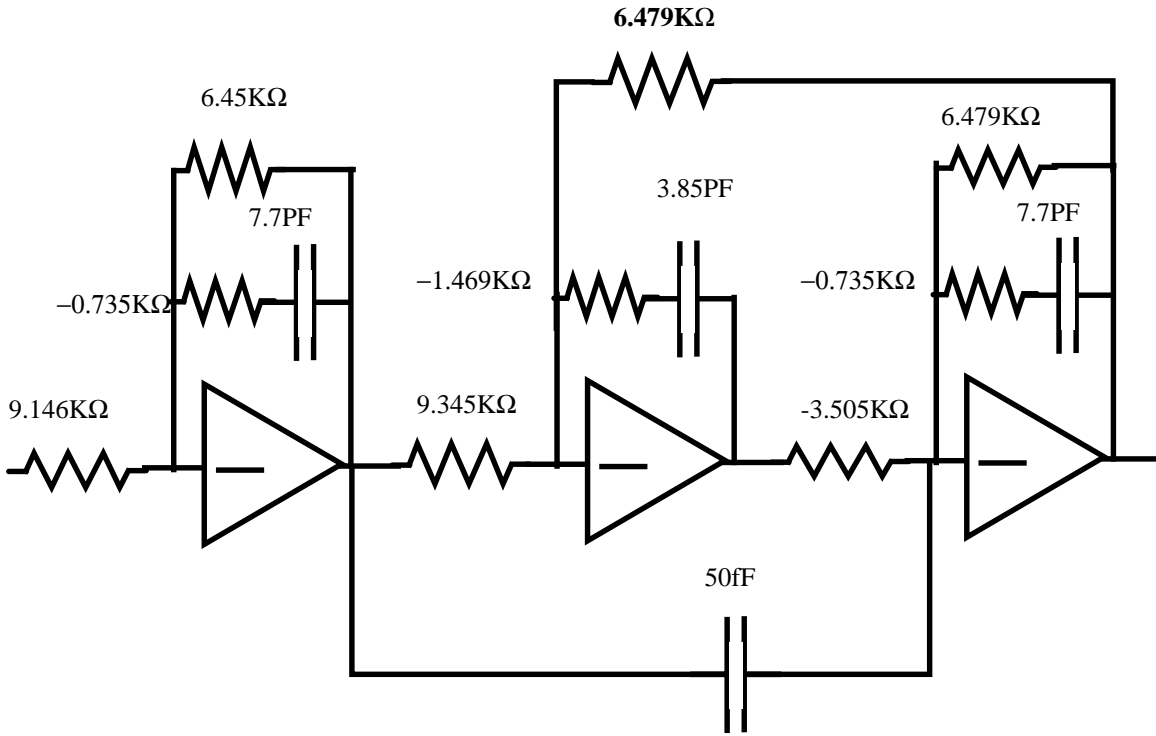


Figure 9: Equivalent single-ended circuit diagram for the 3-rd order elliptic anti-alias filter

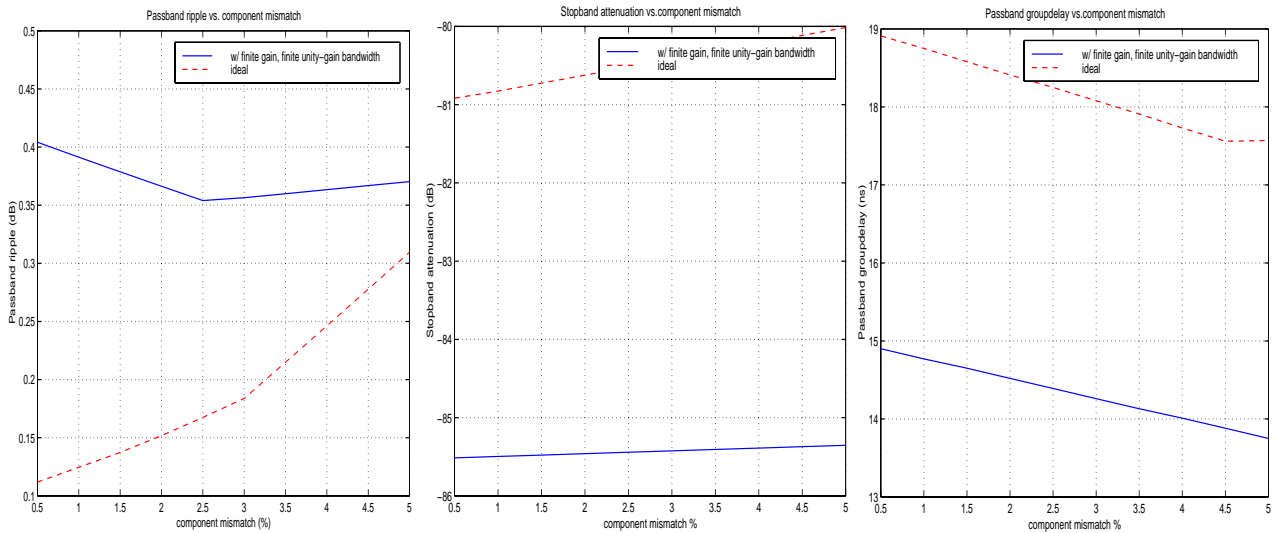


Figure 10: Monte-Carlo analysis for component mismatch. Each data point is extracted from 100 Monte-Carlo simulation runs. Simulation also includes global process variation, which is $\Delta R/R = \pm 20\%$, $\Delta C/C = \pm 10\%$. Both circuits of ideal opamp and of nonideal opamp with pole-zero cancellation are simulated.

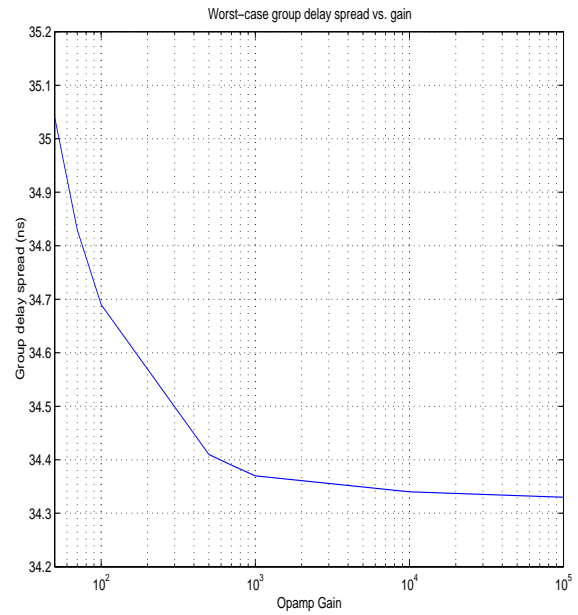
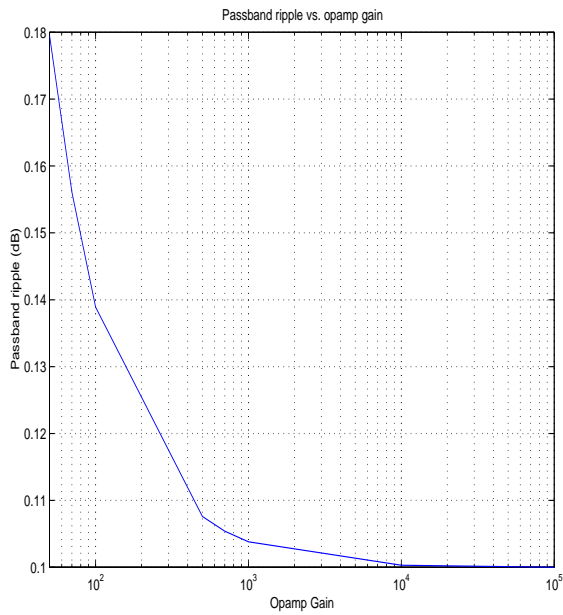


Figure 11: Effect of finite opamp gain.

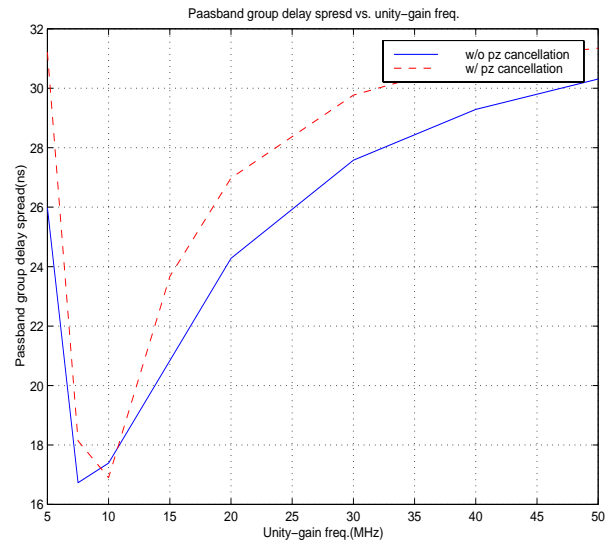
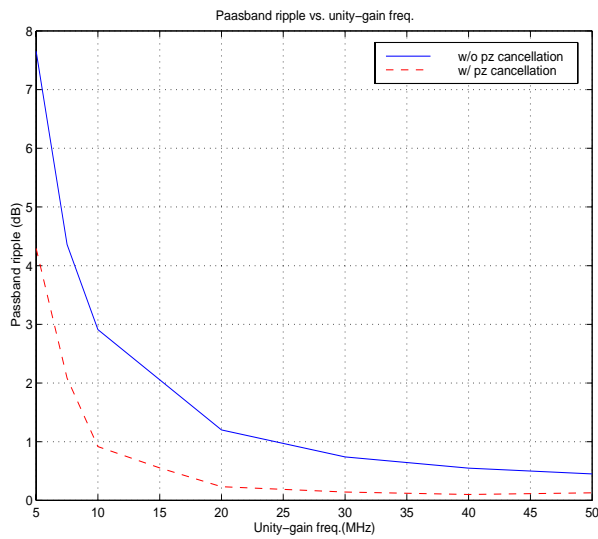


Figure 12: Finite opamp unity-gain bandwidth limitation before and after pole-zero cancellation.

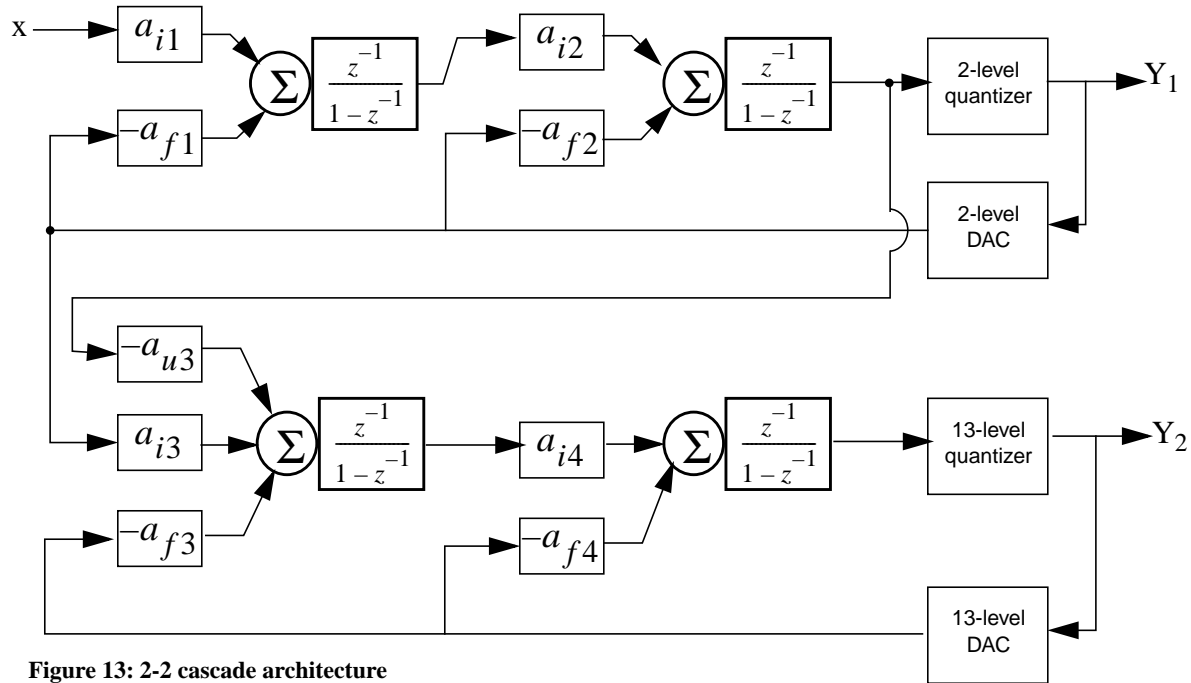


Figure 13: 2-2 cascade architecture

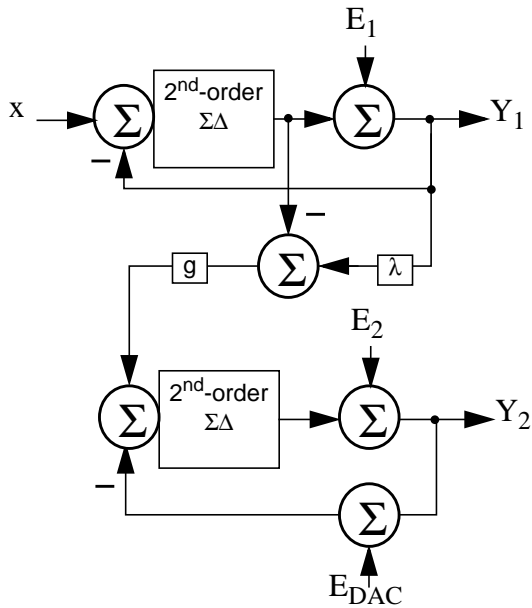


Figure 14: Simplified linear model of 2-2 cascade

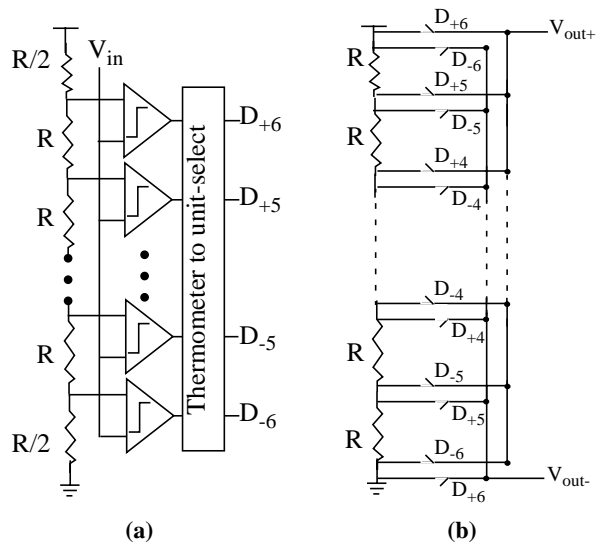
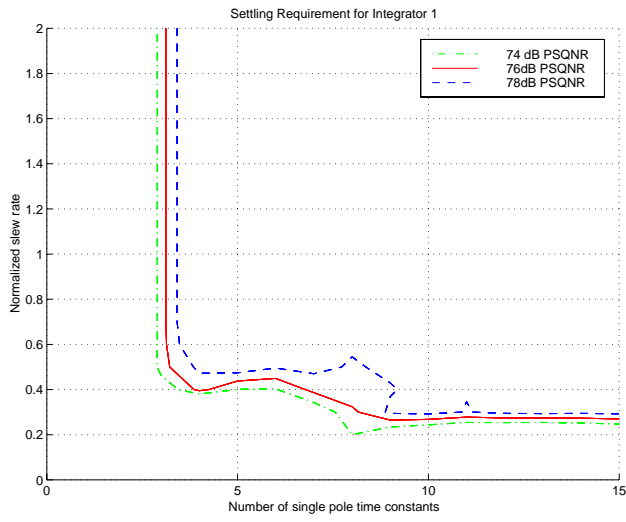
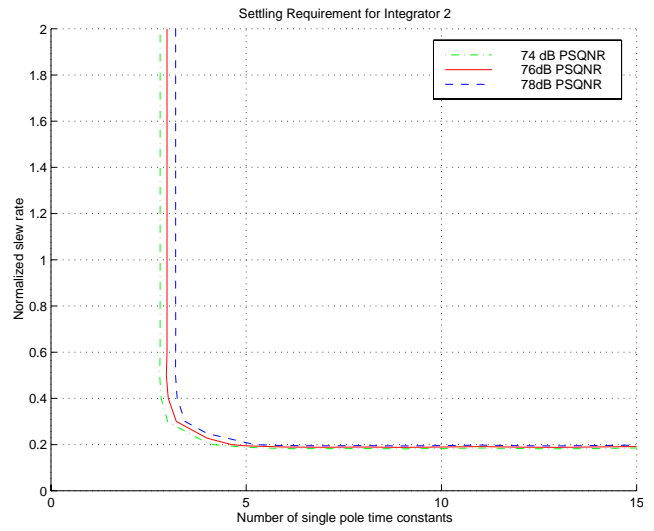


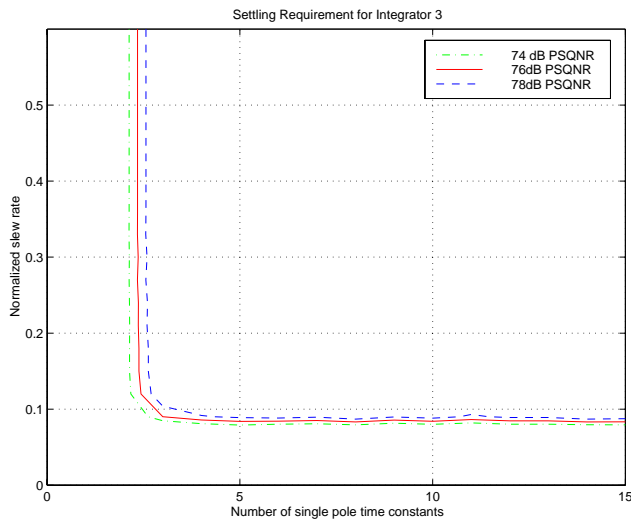
Figure 15: (a) 13-level quantizer (b) 13-level DAC



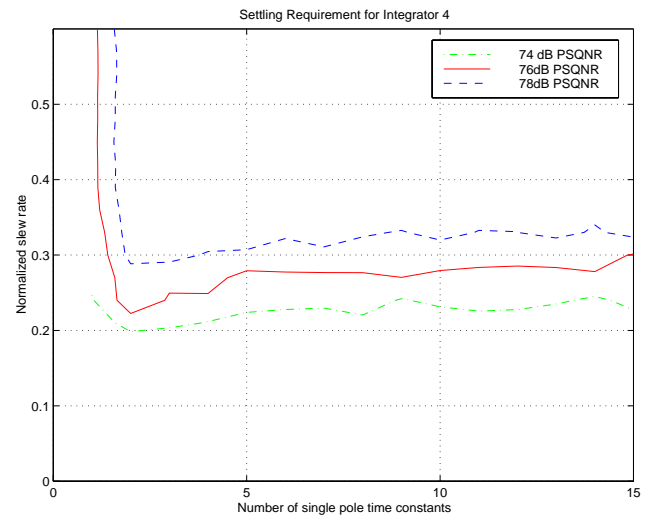
(a)



(b)



(c)



(d)

Figure 16: Settling requirements for (a) integrator 1, (b) integrator 2, (c) integrator 3, (d) integrator 4

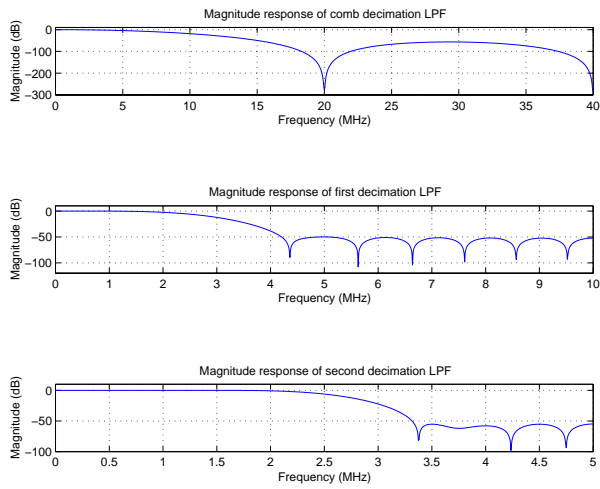


Figure 17: Decimation filter Transfer Functions

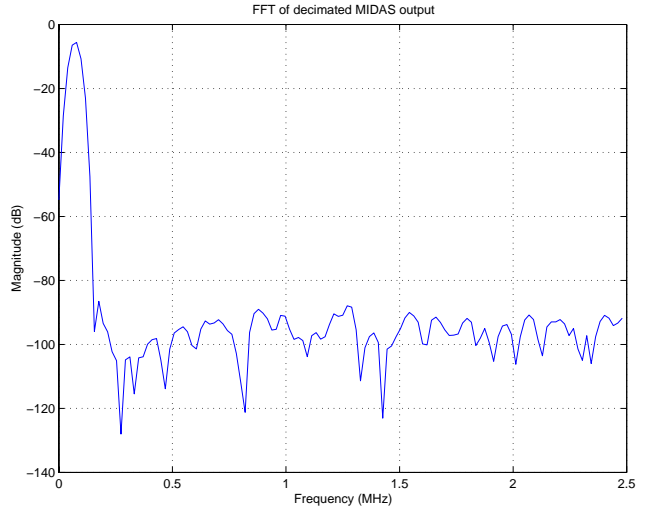


Figure 20: FFT of decimated MIDAS output

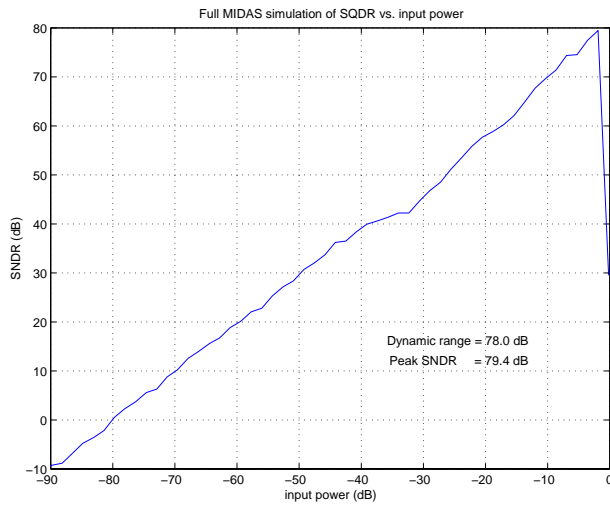


Figure 18: SQDR vs. input amplitude

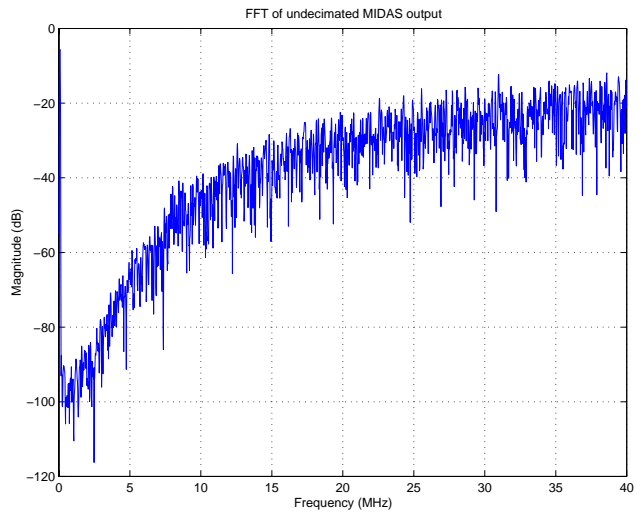


Figure 21: FFT of undecimated MIDAS output

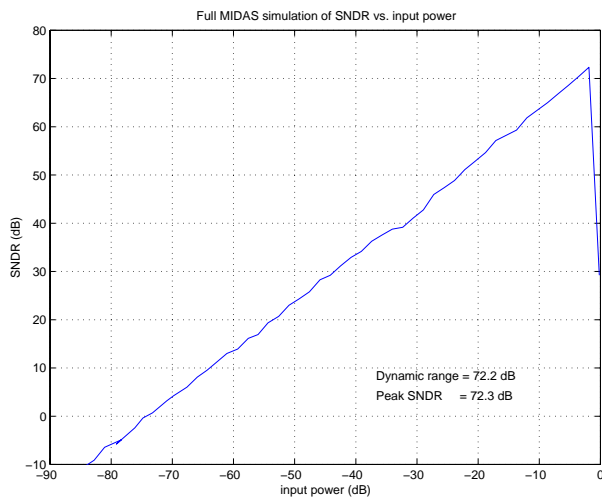


Figure 19: SNDR vs. input amplitude

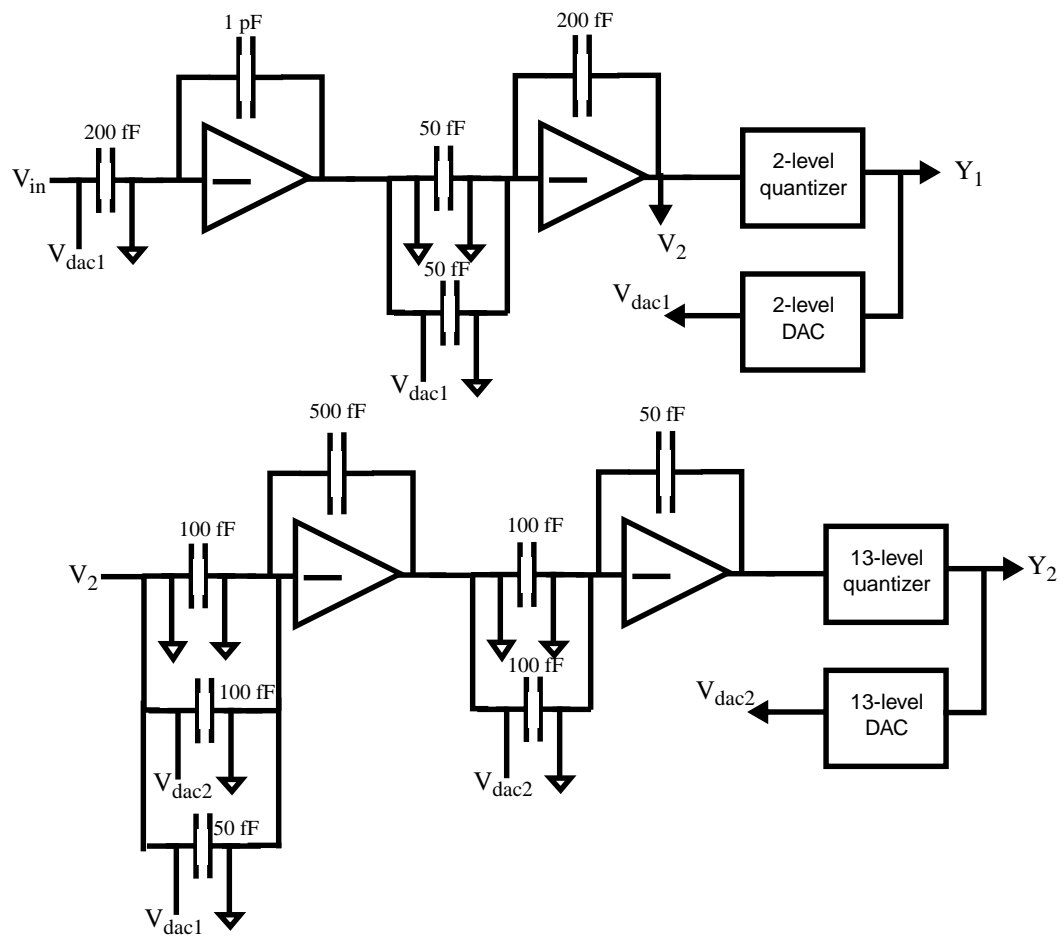


Figure 22: Simplified, single-end equivalent of modulator circuit diagram. (NOTE: All integrators are standard, two-phase full-delaying; switches are not drawn for ease of viewing.)

Table 1 Dynamic range calculations for the converter.

S_{transmit}	0 dBm
Path loss (5 meter)	59.4 dB
Shadowing loss	10 dB
S_{ref}	-69.4 dBm
$S_{N,\text{in}}$	-106.8 dBm
Eb/No required	15 dB
NF_{max}	22.4 dB
$S_{NBB,\text{in}}$	-94.4 dBm
S_{blocker}	-33 dBm
G	41 dB
S_{NBB}	-53.4 dBm, -66.4 dBV
DR	71.4 dB

Table 2 Filter type and order vs. process variation and passband ripple

Bandedge shift Δf_p Δf_{stop} Rp (dB)	$\Delta = \pm 5 \%$			$\Delta = \pm 10 \%$			$\Delta = \pm 30 \%$		
	0.1	1	2	0.1	1	2	0.1	1	2
Butter	4	3	3	4	3	3	4	4	4
Cheb1	3	3	3	3	3	3	4	3	3
Cheb2	3	3	3	3	3	3	4	3	3
elliptic	3	3	3	3	3	3	3	3	3

Table 3 Order, Number of Quantizer bits vs. OSR for given dynamic range

Modulator order	Bits in quantizer	OSR for 80 dB	OSR for 90 dB	OSR for 100 dB
3	1	27	37	52
3	2	20	27	38
3	3	16	22	30
3	4	13	17	24
4	2	13	17	21
4	3	11	14	18
4	4	9	12	15
5	2	10	12	15
5	3	9	11	13
5	4	8	9	11

Table 4 2-2 cascade coefficients

ai1	af1	ai2	af2	au3	ai3	af3	ai4	af4
0.2	0.2	0.5	0.25	0.5	0.1	0.2	4	2

Table 5 Required settling performance and total sampling capacitance for each integrator

Integrator	Normalized Slew Rate	Slew Rate (V/μs)	Number of τ's in T_{settle}	Opamp f_u (MHz)	Total Sampling Capacitance
1 (option 1)	0.35	252	11	350	200 fF
1 (option 2)	0.6	432	5	160	200 fF
2	0.25	180	4	128	100 fF
3	0.1	72	4	128	250 fF
4	0.35	252	3	95	200 fF