CMOS Low Noise Amplifier Design for Wireless Sensor Networks

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Research Project

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1

Introduction

1.1 Motivation

Recently, there has been much research aimed at achieving autonomous wireless sensor nodes. One such project is the PicoRadio project at UC Berkeley, which envisions the sensor nodes collecting data such as temperature, humidity, etc, while scavenging energy from the nearby building environment [1]. In order for the PicoRadio project to attain its goals, a low power transceiver is needed. A major component in the receiver is the low noise amplifier. The low noise amplifier needs to provide an input impedance match as well as amplify the signal without adding too much noise or distortion while consuming minimal power.

1.2 Thesis Organization

In this report, the design and implementation of a low power CMOS LNA is documented. Chapter 2 presents background information about two-port networks that is useful in the design of low noise amplifiers as well as other RF circuits. In chapter 3, more background information is shown, but the focus shifts solely to the design of CMOS low noise amplifiers. Chapter 4 discusses the design of on-chip spiral inductors, which are a

very important component in narrowband LNAs. Chapter 5 builds upon the background information from the previous chapters and documents the design procedure of a low power CMOS LNA. Chapter 6 presents the experimental measurement results of a prototype LNA and an on-chip spiral inductor. Finally, chapter 7 discusses the lessons learned from the research, as well as possibilities for future work.

2

Two-Port Networks

2.1 Introduction

In the design of analog circuits, it is useful to abstract circuit blocks into two-port networks, and it is the purpose of this chapter is to introduce their properties. It begins with a discussion of parameters that are used to characterize two-port networks. Next, figures of merit in two-port networks such as gain, noise, linearity, and stability that are important in the design of low noise amplifiers are presented.

2.2 Representation of Two-Port Networks

As shown in figure 2.1, a two-port network with four terminals and two ports are used to define the input and output of a circuit. Two terminals define a port if the current flowing into one terminal is the same as the current flowing out of the other terminal [2]. At each port there are two variables (voltage and current), one of which will be independent, while the other will be dependent on the two-port network and the independent variables. At low frequencies, two common representations are the impedance matrix (Z parameters) and the admittance matrix (Y parameters).

Figure 2.1. Two-port network diagram

The impedance and admittance matrices are defined by equations 2.1 and 2.2.

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{2.1}$$

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{2.2}$$

Z parameters and Y parameters are particularly useful at low frequencies because they can be measured by applying either a test current or voltage to the input port and connecting either the output port as a short or open circuit, depending on the definition. However, at RF and microwave frequencies, Z and Y parameters become very difficult to measure due to the need for broadband short and open circuits [3]. Furthermore, an active two-port network might oscillate if one of its ports was short or open circuited. As a result, a different representation of the two-port network is needed at RF and microwave frequencies. The representation that is used is the scattering, or S, parameters, and is the topic of the next section.

2.3 Scattering Parameters

Instead of relying on ports being open and short circuited, S parameters have the advantage that they can be measured by matching the source and load impedances to the

reference impedance. A diagram of an S parameter representation of a two-port network is shown in figure 2.2.

Figure 2.2. S parameter representation of a two-port network

The basic idea behind this representation is to measure the normalized incident voltage wave a_i entering the system at port *i*, as well as the corresponding reflected voltage wave b_i leaving port *i*. The normalized incident and reflected voltage waves a_i and b_i are related to the terminal voltage and currents at port *i* by the following equations:

$$a_i = \frac{v_i + Z_o i_i}{2\sqrt{Z_o}} \tag{2.3}$$

$$b_i = \frac{v_i - Z_o i_i}{2\sqrt{Z_o}} \tag{2.4}$$

where Z_o is the reference impedance (assumed real in this analysis, and usually equal to 50 Ω). For the network shown in figure 2.2, the contributions from the two ports can be combined to form equation 2.5 (in matrix form).

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.5}$$

where S_{11}, S_{12}, $S_{21,}$ S_{22} are the scattering parameters measured across ports 1 and 2. By expanding the scattering matrix, the following equations can be written:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2 = 0} \tag{2.6}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1 = 0} \tag{2.7}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2 = 0} \tag{2.8}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1 = 0} \tag{2.9}$$

where S_{11} is interpreted as the ratio between the reflected voltage wave and the incident voltage wave at port 1 with the output port properly terminated. The condition for a port being properly terminated is that its load impedance must match the characteristic impedance. The output or input impedance of the two-port network does not have to match the characteristic impedance. Definitions for the rest of the S parameters can be interpreted analogously.

2.3.1 Conversion to Other Two-Port Network Parameters

Even though measurements of two-port networks at RF frequencies are performed using its S parameters, it is sometimes convenient to represent two-port networks by its Z or Y parameters. For example, to find the relationship between Z and S parameters, first use the definition of Z parameters from equation 2.1 to obtain:

$$V^{+} + V^{-} = Z\left(I^{+} + I^{-}\right) \tag{2.10}$$

where the (+) represents the incident voltage or current, and the (-) notation represents the reflected voltage or current. If Z_o is assumed to be real, then it is equal to a diagonal matrix with value Z_o in the diagonals and zeros elsewhere. Using this fact, and rearranging 2.10, the following equation is obtained.

$$\left(Z + Z_o\right)I^{-} = I^{+}\left(Z - Z_o\right) \tag{2.11}$$

Now, if we apply the definition for S parameters from equation 2.5 and solve for the Z matrix, we arrive at equation 2.12.

$$Z = Z_o\left(1 + S\right)\left(1 - S\right)^{-1} \tag{2.12}$$

where 1 in equation 2.12 is the unit diagonal matrix. [4] conveniently tabulates conversions between other parameters.

2.4 Gain of Two-Port Networks

Analog circuit designers usually think of gain in terms of voltage gain. However, in RF and microwave design, it is usually more helpful to express the gain of a two-port network as power gain. Before embarking on a discussion of power gain, it is first necessary to introduce the maximum power transfer theorem.

2.4.1 Maximum Power Transfer Theorem

RF and microwave designers often refer to a source and load as being "power matched." By "power match," they actually mean that for a given source impedance, the load impedance is such that the maximum available power is being transferred to the load from the source.

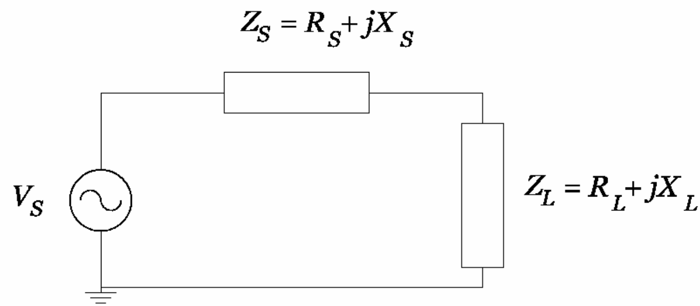


Figure 2.3. Simple network for maximum power transfer theorm

Consider the circuit shown in figure 2.3. The power delivered to the load is entirely due to R_L, and is equal to:

$$P_L = \frac{\left|V_{RL}{}^2\right|}{R_L} = \frac{R_L \left|V_S\right|^2}{\left|Z_L + Z_S\right|^2} \tag{2.13}$$

Separating the real and imaginary parts of the impedances gives the result shown in equation 2.14.

$$P_L = \frac{\left|V_{RL}{}^2\right|}{R_L} = \frac{R_L \left|V_S{}^2\right|}{(R_L + R_S)^2 + (X_L + X_S)^2} \tag{2.14}$$

From equation 2.14, it can be seen that the power to the load is maximized when (X_L + X_S) = 0 and R_L = R_S, or in other words, when Z_L and Z_S are complex conjugates. Another observation is that the maximum amount of power the source can transfer to the load is only half of the amount available.

2.4.2 Gain Expressions

If the two-port network shown in figure 2.4 is considered, many useful gain expressions can be defined in terms of the different reflection coefficients and the two-port s-parameters.

Figure 2.4. Two port network reflection coefficients

The reflection coefficient is the ratio between the reflected voltage wave from a port and the incident voltage wave entering the port, and is given by equation 2.15.

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \tag{2.15}$$

The following equations introduce the definitions of the power gains of two-port networks [5]:

$$G_T = \frac{P_L}{P_{AVS}} \tag{2.16}$$

$$G_P = \frac{P_L}{P_{IN}} \tag{2.17}$$

$$G_A = \frac{P_{AVN}}{P_{AVS}} \tag{2.18}$$

G_T is referred to as the transducer power gain, and is probably the most meaningful gain metric. The transducer power gain represents the power that is delivered to the load (load mismatch) given the power available from the source (source mismatch). G_P is the power gain, and is the power that is delivered to the load (load mismatch) from the power input to the network. G_A is the available power gain, and it represents the power available from the network (matched load) given the power available from the source (source mismatch). From these above definitions, it is worthwhile to notice that G_T will always be less than or equal to G_P, and G_T will always be less than or equal to G_A. However, if the source and load are both conjugate matched to the input and output impedance of the two-port network, then all the power gains will be equal.

Using the definitions introduced in equations 2.15 – 2.18, the different gain expressions can be derived.

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{IN}\Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \tag{2.19}$$

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{OUT}\Gamma_L|^2} \tag{2.20}$$

$$G_P = \frac{1}{1 - |\Gamma_{IN}|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \tag{2.21}$$

$$G_A = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} |S_{21}|^2 \frac{1}{1 - |\Gamma_{OUT}|^2} \tag{2.22}$$

where the different reflection coefficients are defined in equation 2.15. If Z_{IN} and Z_{OUT} are not known, then it is necessary to use the alternate expressions for Γ_{IN} and Γ_{OUT} given in equation 2.23 and 2.24.

$$\Gamma_{IN} = S_{11} + \frac{S_{12} S_{21} \Gamma_L}{1 - S_{22} \Gamma_L} \tag{2.23}$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12} S_{21} \Gamma_S}{1 - S_{11} \Gamma_S} \tag{2.24}$$

It is also useful to define the voltage gain as:

$$A_V = \frac{V_{OUT}}{V_{IN}} \tag{2.25}$$

Using the above definition, an expression for the voltage gain is shown below.

$$A_V = \frac{S_{21}(1 + \Gamma_L)}{(1 - S_{22}\Gamma_L) + S_{11}(1 - S_{22}\Gamma_L) + S_{21}\Gamma_L S_{12}} \tag{2.26}$$

2.5 Noise in Two-Port Systems

Before beginning an analysis of noise, it is necessary to first introduce the definition of the noise factor (noise figure is noise factor expressed in dB).

$$F = \frac{SNR_{IN}}{SNR_{OUT}} = \frac{P_{noise,output}}{G_p P_{noise,source}} \tag{2.27}$$

where G_p is the power gain of the two-port network. The noise factor is a measure of the amount of noise a two-port network adds, and is the equal to the ratio between the total

output noise power and the output noise power due to the input source. An ideal noiseless two-port network contributes no noise, and the noise factor is equal to one.

In the analysis of noise in two-port systems, first consider a noisy two-port network being driven by a noisy source as shown in figure 2.5a. The noise of the two-port network can be input referred as a noise voltage and noise current to form the equivalent circuit shown in figure 2.5b.

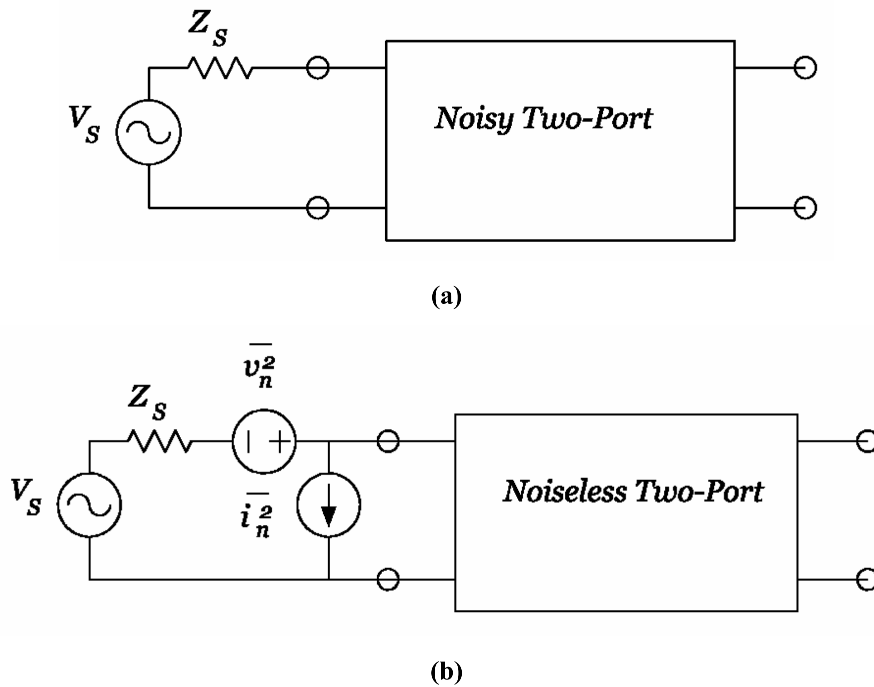


Figure 2.5. (a) Noisy two-port. (b) Equivalent model

Since the noise of the two-port network was referred to the input, the noise factor can be directly calculated, and is equal to [6]:

$$F = \frac{\overline{i_s^2} + \overline{\left| i_n + Y_s v_n \right|^2}}{i_s^2} \tag{2.28}$$

In writing down equation 2.28, the assumption was made that the noise from the source is not correlated to the noise from the two-port network. However, since the exact nature of

the source of the two-port network is not known, no assumptions about its correlation can be made. Therefore, the following definition is needed for i_n.

$$i_n = i_c + i_u \tag{2.29}$$

In equation 2.29, i_c is the portion of i_n that is correlated with v_n, while i_u is the part of i_n that is uncorrelated with v_n.

Before continuing, the following definitions in equations 2.30 – 2.33 are made to facilitate the derivation.

$$Y_c \equiv \frac{i_c}{v_n} \tag{2.30}$$

$$R_n \equiv \frac{\overline{v_n^{\,2}}}{4kT\,\Delta f} \tag{2.31}$$

$$G_u \equiv \frac{\overline{i_u^{\,2}}}{4kT\,\Delta f} \tag{2.32}$$

$$G_s \equiv \frac{\overline{i_s^{\,2}}}{4kT\,\Delta f} \tag{2.33}$$

Using equations 2.30 – 2.33, the noise factor can be re-written as:

$$F = 1 + \frac{G_u + \left|Y_c + Y_s\right|^2 R_n}{G_s} \tag{2.34}$$

which simplifies to:

$$F = 1 + \frac{G_u + [(G_c + G_s)^2 + (B_c + B_s)^2]R_n}{G_s} \tag{2.35}$$

The minimum noise factor can be solved for by first taking the derivative of equation 2.35 with respect to the source conductance and susceptance and setting them equal to zero.

The results for the optimal source conductance and susceptance are stated below.

$$B_{s,opt} = -B_c \tag{2.36}$$

$$G_{s,opt} = \sqrt{\frac{G_u}{R_n} + G_c^{\,2}} \tag{2.37}$$

Substituting equations 2.36 and 2.37 into 2.35 gives the following result for the minimum noise figure.

$$F_{\min} = 1 + 2R_n(G_{s,opt} + G_c) \tag{2.38}$$

With the aid of equation 2.38, the general expression for noise figure is:

$$F = F_{\min} + \frac{R_n}{G_s}[(G_s - G_{s,opt})^2 + (B_s - B_{s,opt})^2] \tag{2.39}$$

From equation 2.39, it can be seen that contours of constant noise factor (and noise figure) are circles centered about ($G_{s,opt}$, $B_{s,opt}$).

The above analysis shows that a minimum noise figure exists for an optimal source impedance, but that the source impedance that optimizes for noise is often not the same as the impedance that achieves maximum power transfer.

2.6 Linearity

In the previous section, noise in two-port systems was examined. In this section, another non-ideality, linearity, is presented. Ideally, two-port networks are linear, and in many analyses this assumption is made because the input signal is small enough such that the non-linear effects of the two-port network can be ignored. However, in LNA design, linearity is a key issue because the LNA must be able to maintain linear operation even in the presence of large input signals [7].

2.6.1 Harmonic Distortion

If a memoryless two-port network shown is assumed, then the output and input can be related by a power series [8].

$$S_o = a_1 S_i + a_2 S_i^2 + a_3 S_i^3 + \ldots \tag{2.40}$$

where a_1, a_2, a_3, are constants. Now, if a sine wave drive is applied to the input, as shown by equation 2.41,

$$S_i(t) = S_1 \cos(\omega_1 t) \tag{2.41}$$

then the output will be equal to:

$$\begin{aligned} S_o(t) = a_1 S_1 \cos(\omega_1 t) + \frac{a_2 S_1^2}{2}[\cos(2\omega_1 t) + 1] \\ + \frac{a_3 S_1^3}{4}[\cos(3\omega_1 t) + 3\cos(\omega_1 t)] + \ldots \end{aligned} \tag{2.42}$$

The first term in equation 2.42 is the linear term, and is what S_o ideally would be equal to if the two-port network was completely linear. The rest of the terms in equation 2.42 are due to non-linearities, and they cause harmonic distortion terms at $2\omega_1$, $3\omega_1$, … as well as

a DC shift, and either gain compression or gain expansion (depending on the sign). It can also be observed from equation 2.42 that distortion is present in any real circuit at any signal level.

To quantify the amount of harmonic distortion, the following definitions are used:

$$HD_2 = \frac{Amplitude_{2\omega 1}}{Amplitude_{\omega 1}} \tag{2.43}$$

$$HD_3 = \frac{Amplitude_{3\omega 1}}{Amplitude_{\omega 1}} \tag{2.44}$$

where equation 2.43 represents the fractional second harmonic distortion, and equation 2.44 represents the third fractional harmonic distortion. Higher order fractional harmonic distortion definitions can be written in the same fashion.

The above definitions for the second and third order fractional harmonic distortion can be written in terms of the coefficients of the power series and the input signal by examining equation 2.42.

$$HD_2 = \frac{a_2}{2a_1} S_1 \tag{2.45}$$

$$HD_3 = \frac{a_3}{4a_1} S_1^2 \tag{2.46}$$

2.6.2 Intermodulation

Previously, harmonic distortion was introduced as the result of non-linearities due to a single sinusoidal input. When two or more sine waves are applied to the input of a two-port network, another non-linearity called intermodulation also occurs. To see the effects of both harmonic distortion and intermodulation, assume that the input signal is now equal to:

$$S_i(t) = S_1 \cos(\omega_1 t) + S_2 \cos(\omega_2 t) \tag{2.47}$$

The output can be expanded in a power series, and equation 2.47 can be substituted into equation 2.40. Once again, the linear first term will be obtained:

$$a_1 S_i = a_1 [S_1 \cos(\omega_1 t) + S_2 \cos(\omega_2 t)] \tag{2.48}$$

The second term is now:

$$\begin{aligned} a_2 S_i^2 = {} & \frac{a_2 S_1^2}{2}[\cos(2\omega_1 t) + 1] + \frac{a_2 S_2^2}{2}[\cos(2\omega_2 t) + 1] \\ & + a_2 S_1 S_2 [\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t] \end{aligned} \tag{2.49}$$

Expanding the third term gives:

$$\begin{aligned} a_3 S_i^3 = {} & \frac{a_3 S_1^3}{4}[\cos(3\omega_1 t) + 3\cos(\omega_1 t)] \\ & + \frac{a_3 S_2^3}{4}[\cos(3\omega_2 t) + 3\cos(\omega_2 t)] \\ & + \frac{3}{4} a_3 S_1 S_2^2 [2\cos(\omega_1 t) + \cos(2\omega_2 + \omega_1)t + \cos(2\omega_2 - \omega_1)t] \\ & + \frac{3}{4} a_3 S_1^2 S_2 [2\cos(\omega_2 t) + \cos(2\omega_1 + \omega_2)t + \cos(2\omega_1 - \omega_2)t] \end{aligned} \tag{2.50}$$

It can be observed from equations 2.49 and 2.50 that harmonic distortion terms are produced as if each sine wave was applied separately. However, second order intermodulation terms are also produced at $(\omega_1 + \omega_2)$ and $(\omega_1 - \omega_2)$, and third order intermodulation terms are produced at $(2\omega_1 \pm \omega_2)$, and $(2\omega_2 \pm \omega_1)$. Figure 2.6 shows the frequency positions of the distortion terms.

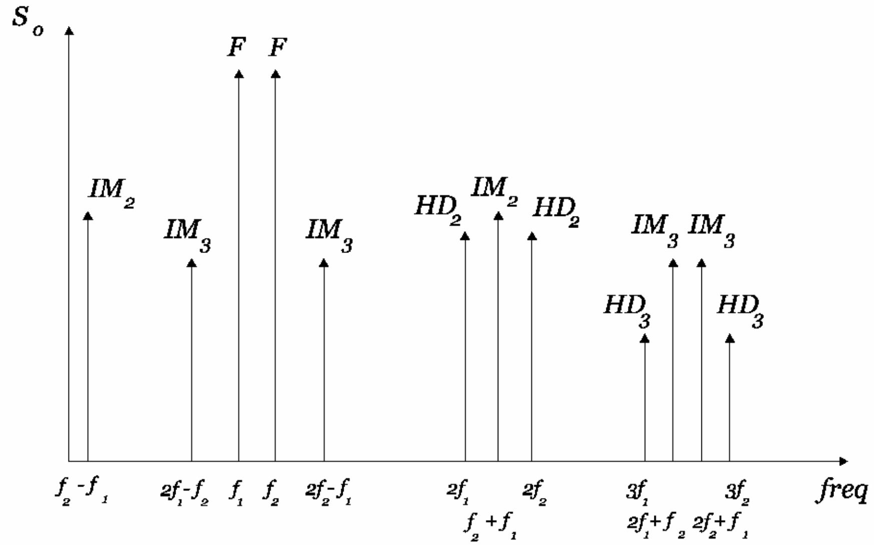


Figure 2.6. Frequency locations of distortion terms

The following two equations define fractional intermodulation:

$$IM_2 = \frac{Amplitude_{\omega_1 \pm \omega_2}}{Amplitude_{\omega_1, \omega_2}} \tag{2.51}$$

$$IM_3 = \frac{Amplitude_{(2\omega_1 \pm \omega_2), (2\omega_2 \pm \omega_1)}}{Amplitude_{\omega_1, \omega_2}} \tag{2.52}$$

Using the definitions presented in equations 2.51 and 2.52, the fractional intermodulation terms are:

$$IM_2 = \frac{a_2}{a_1} S_1 \tag{2.53}$$

$$IM_3 = \frac{3a_3}{4a_1} S_1^{\,2} \tag{2.54}$$

where it was assumed that $S_1 = S_2$.

2.6.3 1 dB Compression Point

It was mentioned previously that the third order term in the power series can either cause gain compression or gain expansion depending on its sign. If we assume that the sign between a_1 and a_3 are different, then gain compression will occur, and the 1 dB compression point can be measured. The 1 dB compression point (P_{-1dB}) is a measure of the power of the input signal such that it causes the 3rd order non-linearity to decrease the linear gain by 1 dB. The previous statement translates mathematically to equation 2.55.

$$20\log\left(1+\frac{3a_3}{4a_1}S_1^{\ 2}\right) = -1\ dB \tag{2.55}$$

Solving for S_1 in equation 2.55 gives:

$$P_{-1dB} = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|}\sqrt{0.11} \tag{2.56}$$

2.6.4 3rd Order Intercept Point

Another measure of the amount of 3rd order non-linearity in a two-port network is the 3rd order intercept point. Since the 3rd order non-linearity is proportional to the input signal cubed, while the fundamental is increasing only linearly with input signal, there will be a point at which the amplitudes of the fundamental and the 3rd intermodulation meet. The input signal, S_1, at which this occurs is defined as the input-referred 3rd order intercept point (IIP_3), and is equal to when IM_3 equals 1. Solving for S_1 using equation 2.54, the following equation for IIP_3 is obtained.

$$IIP_3 = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|} \quad (2.57)$$

2.7 Stability

One important property of two-port networks is that it must not be susceptible to unwanted oscillation. This means that the input and output resistance of the two-port network must never be negative in the presence of different values for the source and load impedance. The stability of a two-port network can be determined from its S-parameters and the load and source impedances. For a two-port network to be unconditionally stable, the following four conditions must be satisfied:

$$\left|\Gamma_S\right| < 1 \quad (2.58)$$

$$\left|\Gamma_L\right| < 1 \quad (2.59)$$

$$\left|\Gamma_{IN}\right| < 1 \quad (2.60)$$

$$\left|\Gamma_{OUT}\right| < 1 \quad (2.61)$$

where Γ_{IN} and Γ_{OUT} are defined in equations 2.23 and 2.24. From equations 2.58 – 2.61, a metric that measures the stability of a two-port network can be derived. (See [9] for derivation.) The result is the Rollet stability factor, K, and unconditional stability is satisfied under the following two conditions:

$$K > 1 \quad (2.62)$$

$$\Delta < 1 \quad (2.63)$$

where

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{2.64}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.65}$$

However, K alone is usually good enough to test for stability since most transistors will either be unconditionally stable or conditionally stable with $K < 1$ and $|\Delta| < 1$ [10]. If a two-port network is potentially unstable with $0 < K < 1$, then most of the Smith Chart is stable, whereas if $K < 0$, then most of the Smith Chart is unstable.

3

CMOS LNA Fundamentals

3.1 Introduction

Even though CMOS technology has been used in digital circuits and low-frequency analog circuits for many years, it is only within the early nineties that research has shown that CMOS is capable of being used in RF circuits [11] [12]. With the backend of transceivers already being implemented in CMOS, it is attractive to use CMOS in the RF frontend in order to integrate the receiver on a single chip. This chapter introduces basic concepts and design considerations associated with CMOS LNAs.

3.2 Impedance Matching

Impedance matching is important in LNA design because often times the system performance can be strongly affected by the quality of the termination [13]. For instance, the frequency response of the antenna filter that precedes the LNA will deviate from its normal operation if there are reflections from the LNA back to the filter. Furthermore, undesirable reflections from the LNA back to the antenna must also be avoided. The quality of the termination is defined by the reflection coefficient Γ introduced in chapter

2. An impedance match is when the reflection coefficient is equal to zero, and occurs when $Z_S = Z_L$ in figure 3.1.

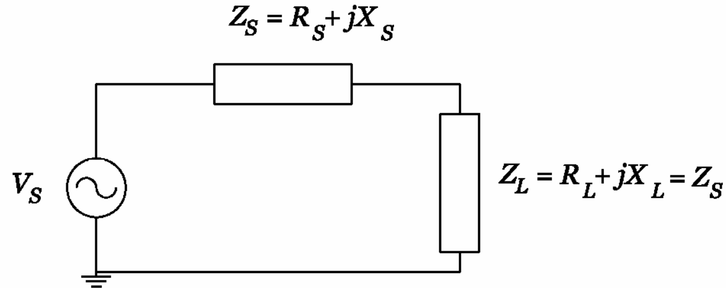


Figure 3.1. Condition for an Impedance Match

There is a subtle difference between impedance matching and power matching. As stated in the previous paragraph, the condition for impedance matching occurs when the load impedance is equal to the characteristic impedance. However, the condition for power matching occurs when the load impedance is the complex conjugate of the characteristic impedance. When the impedances are real, the conditions for power matching and impedance matching are equal.

3.3 Non-Quasi Static Effect

An important consideration that needs to be taken into account in the design of narrowband CMOS LNAs is the non-quasi static effect. As later sections will show, the non-quasi static effect imposes limits on noise and gain performance. The goal of this section is to introduce this phenomenon by revealing its physical origins, presenting a first order model, and discussing its importance.

3.3.1 Physical Origins

In order to understand the non-quasi static effect, it is important to first look at the assumption that MOS transistors operating at low frequencies ($\omega << \omega_T$) can be modeled only by a capacitance from gate to source. (Figure 3.2)

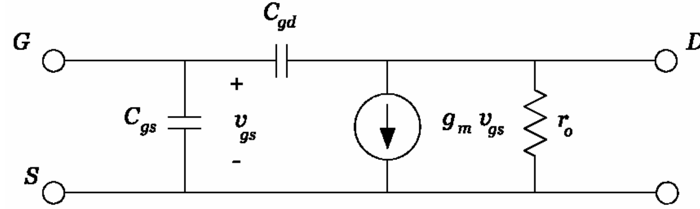


Figure 3.2. Simple small signal model for MOS at low frequencies

The reason that this model is accurate at low frequencies is because the inversion layer channel charge builds up fast enough relative to the frequency of the signal applied a terminal. However, at high frequencies this assumption can no longer be made due to the finite channel conductance limiting the speed of the build-up of the inversion layer. As a result, the channel needs time to achieve equilibrium with the source and drain voltages. This high frequency phenomenon is called the non-quasi static effect.

3.3.2 First Order Model

Figure 3.3a presents a small-signal non-quasi static equivalent circuit model proposed in [14]. However, for most practical purposes, this model can be simplified to that shown in figure 3.3b by approximating the time constant τ_1 in the transconductor with (τ_1 - τ_2) by taking v_{gc} instead of v_{gs}, where τ_1 and τ_2 are equal to

$$\tau_1 = \frac{2}{5\omega_T}\frac{1+3\eta+\eta^2}{(1+\eta)^3} \tag{3.1}$$

$$\tau_2 = \frac{1}{5\omega_T} \frac{2 + 8\eta + 5\eta^2}{(1+\eta)^2(1+2\eta)} \tag{3.2}$$

and η is given as:

$$\eta = \begin{cases} 1 - \alpha \dfrac{V_{DS}}{V_{GS} - V_T} & V_{DS} \leq \dfrac{V_{GS} - V_T}{\alpha} \\ 0 & V_{DS} > \dfrac{V_{GS} - V_T}{\alpha} \end{cases} \tag{3.3}$$

where α is dependent on the surface potential and the body effect and is normally assumed to be equal to 1 [15].

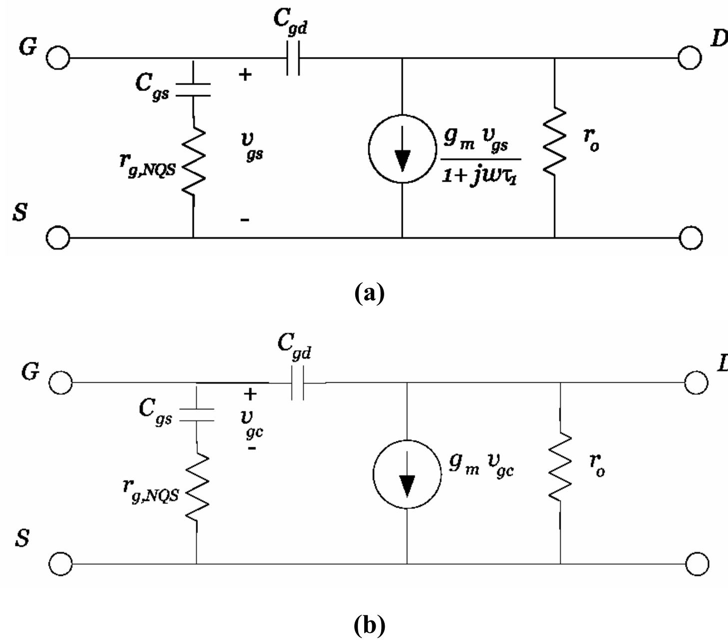


Figure 3.3. First order small signal model including NQS effect. (a) valid in saturation and linear region. (b) valid in saturation only

The NQS model uses an extra resistance in series with the gate to source capacitance to model the non-quasi static effect. This resistance is referred to as the non-quasi static gate resistance, and it is the effective resistance seen by the gate to source

capacitance. The non-quasi static gate resistance in strong inversion is defined by the equation below:

$$r_{g,NQS} = \frac{\tau_1 - \tau_2}{C_{gs}} \tag{3.4}$$

Using equations (3.1) – (3.4), the value of the non-quasi static gate resistance in saturation can be determined, and is given in the equation below:

$$r_{g,NQS} = \frac{1}{5 g_m} \tag{3.5}$$

One final remark about the non-quasi static gate resistance is that the derivation was done for long channel transistors without considering short-channel effects.

3.3.3 Importance of the Non-Quasi Static Effect

It was mentioned that the non-quasi static effect occurs when a high frequency signal is applied to the gate. For most practical circuits, the frequency is low enough such that the imaginary part of the impedance (due to C_{gs}) is much greater than the real part (due to $r_{g,NQS}$). If this is the case, then one might wonder why even model this resistance at all? The answer is that when an inductor is placed in series with C_{gs} (as is often the case in narrowband LNA design), then at the resonance the impedance of the inductor will cancel out the impedance of the capacitor. As a result, with an ideal inductor, the input impedance is solely determined by $r_{g,NQS}$.

3.4 Noise Sources in CMOS

Before beginning an analysis of how to design for low noise, the origins of the noise must be identified and understood. This section gives insight into the two most important noise sources in CMOS transistors.

3.4.1 Thermal Noise

Thermal noise is due to the random thermal motion of the carriers in the channel [16]. It is commonly referred to as a white noise source because its power spectral density holds a constant value up to very high frequencies (over 1 THz). Thermal noise is commonly modeled as current source across the drain and the source in shunt with the transconductor of the transistor (figure 3.4).

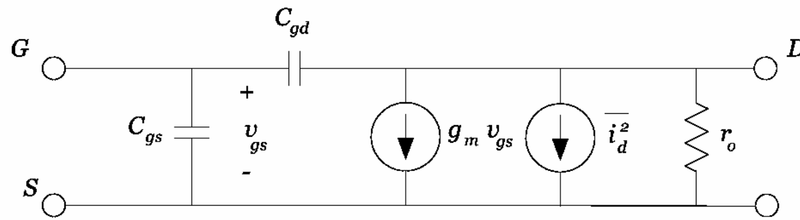


Figure 3.4. Thermal noise small signal circuit model

Thermal noise has a power spectral density given by:

$$\frac{\overline{i_d^{\,2}}}{\Delta f} = 4kT\frac{\mu}{L^2}(-Q_I) \tag{3.6}$$

where k is Boltzmann's constant, T is the absolute temperature, μ is the mobility, L is the transistor length, and Q_I is the total inversion layer charge. Equation 3.6 is suitable for both strong inversion and weak inversion, provided that the appropriate Q_I is used.

When the transistor is in strong inversion, equation 3.6 can be reduced down to:

$$\frac{\overline{i_d^{\,2}}}{\Delta f} = 4kT\gamma g_{ds0} \tag{3.7}$$

where γ is the bias dependent parameter, and g_{ds0} is the zero-V_{DS} drain-source conductance, and has the following definition:

$$\alpha = \frac{g_m}{g_{ds0}} \tag{3.8}$$

where α is between 0 and 1.

Equation 3.7 is a general equation that can be used in both the linear and saturation regions of operation simply by using different values for γ. For long channel transistors, γ = 2/3 in the saturation region, and γ = 1 in the linear region. For short channel transistors, hot carrier effects may cause γ to be as high as 2 or 3 [17].

3.4.2 Induced Gate Noise

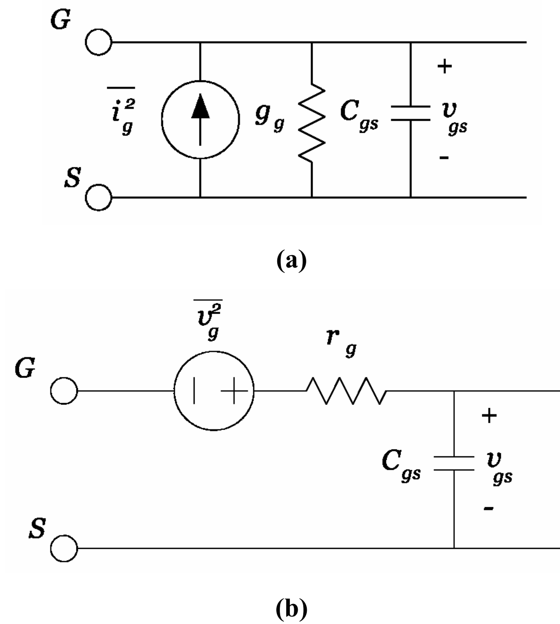


Figure 3.5. Induced gate noise model (a) frequency dependent (b) frequency independent

Induced gate noise is a high frequency noise source that is caused by the non-quasi static effects influencing the power spectral density of the drain current [18]. Thermal noise in the channel couples through the oxide capacitance to the gate terminal, causing a gate

noise current to flow. This noise source is normally not included in standard noise analysis because at low frequencies it is negligible. However, this noise source can dominate at RF frequencies [19]. Induced gate noise has a power spectral density given by equation 3.8, and its circuit model is shown in figure 3.5a.

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta \frac{\omega^2 C_{gs}^2}{5 g_{ds0}} \tag{3.9}$$

where the parameter δ is equal to 4/3 in long channel devices [20]. Since the thermal channel noise and induced gate noise stem from the same physical phenomenon, [21] assumes that the relation $\delta = 2\gamma$ continues to hold for short channel devices.

The power spectral density of equation 3.9 is frequency dependent. An equivalent frequency independent noise model is to express the induced gate noise as a voltage in series with the gate capacitance, as shown in figure 3.5b. If a high Q is assumed, then the models shown in figure 3.5a and b are equivalent, and equation 3.10 gives the power spectral density.

$$\frac{\overline{v_g^2}}{\Delta f} = 4kT\delta r_{g,NQS} \tag{3.10}$$

Equation 3.10 shows the interesting result that the gate noise is equal to the noise of $r_{g,NQS}$, but with an extra parameter δ.

It was mentioned earlier that the gate noise is related to the drain noise. In fact, it is partially correlated to the drain noise, with a correlation coefficient c, stated in equation 3.11 below.

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} \tag{3.11}$$

The value for c is given by [22] as 0.395j for long channel devices. The purely capacitive nature of the correlation coefficient is due to the fact that the coupling between the gate noise and drain noise is through the gate capacitance.

3.4.3 Other Noise Sources

The distributed gate resistance of the CMOS transistor also contributes to the noise in low noise amplifiers. This noise source is modeled as a series resistance with the gate and has a noise power equal to

$$\frac{\overline{v_g^{\,2}}}{\Delta f} = 4kTR_g \tag{3.12}$$

where R_g is the gate resistance, and is equal to

$$R_g = \frac{R_{sq} W}{3n^2 L} \tag{3.13}$$

In equation 3.13, R_{sq} is the sheet resistance of polysilicon, n is the number of fingers, and the factor 3 comes from the distributed nature of the gate resistance assuming that each finger is only contacted at only one end. If both ends are contacted, then then the factor reduces to 12. This noise source can be made negligible by increasing the number of fingers used to make a transistor.

Another noise source mentioned in [23] is from the resistance due to the lightly doped drain diffusion regions. Because no distinction is made between the source and drain, this resistance is also present at the source, and cannot be mitigated by proper layout. This resistance is given in equation 3.14.

$$R_{source\ ,drain} = \frac{R_{LDS}}{W} \tag{3.14}$$

where R_{LDS} is the resistance of a unit width transistor.

3.5 Inductive Source Degeneration

3.5.1 Input Impedance Match

It was mentioned previously that providing an impedance (and power, if the source impedance is real) match was important in LNA design. Input impedance matching by using inductive source degeneration is a very popular approach because matching to the source does not introduce additional noise (as in the case of using a shunt input resistor), and does not restrict the value of g_m (as in the case of the common-gate configuration).

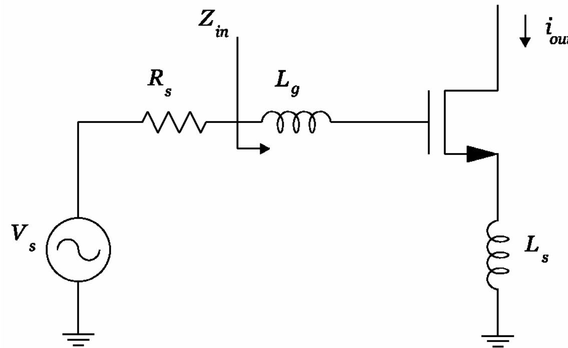


Figure 3.6. Inductive source degeneration

The circuit shown in figure 3.6 has an input impedance equal to

$$Z_{in}(\omega) = j\omega\left(L_s + L_g\right) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} + r_{g,NQS} \tag{3.15}$$

where ideal inductors have been assumed. From equation 3.15, in order to achieve an input match, the following condition must be satisfied.

$$R_s = \frac{g_m L_s}{C_{gs}} + r_{g,NQS} \approx \omega_t L_s + r_{g,NQS} \qquad (3.16)$$

where ω_t is the transition frequency of the transistor. Once L_s is chosen to provide the input match, L_g can be chosen such that Z_{in} is real and equal to equation 3.16 at the resonant frequency ω_o. In other words, the following condition for L_g must hold:

$$\omega_o = \frac{1}{\sqrt{(L_s + L_g)C_{gs}}} \qquad (3.17)$$

3.5.2 Effective Transconductance of Matched Device

To find the transconductance of the circuit shown in figure 3.6, first note that the input matching network forms a series RLC tank. The Q of the tank can be defined as

$$Q_{in} = \frac{1}{\omega_o (R_S + \frac{g_m L_s}{C_{gs}} + r_{g,NQS}) C_{gs}} \qquad (3.18)$$

where ω_o is the resonant frequency defined in equation 3.17. At resonance, the voltage across the capacitor is equal to

$$v_{gs} = Q_{in} v_s \qquad (3.19)$$

and the short circuit output current is equal to

$$i_{out} = g_m v_{gs} \qquad (3.20)$$

where g_m is the intrinsic transconductance of the device. Using equations 3.18 – 3.20, the overall transconductance can be solved for, and is given by the following equation:

$$G_m = \frac{g_m}{\omega_o (R_S + \frac{g_m L_s}{C_{gs}} + r_{g,NQS})C_{gs}}$$

$$\approx \left(\frac{\omega_t}{\omega_o}\right)\frac{1}{(R_S + \omega_t L_s)} \tag{3.21}$$

It can be observed from equation 3.21 that the effective transconductance is independent of the g_m of the device, and is dependent on CMOS process technology through the transition frequency.

An alternate way of solving for the effective transconductance is to transform the source into its Norton equivalent. Therefore, the current flowing through C_{gs} is equal to

$$i_{gs} = \frac{i_{in}}{2R_S} \tag{3.22}$$

and v_{gs} is equal to

$$v_{gs} = \frac{i_{in}}{2R_S}\frac{1}{j\omega_o C_{gs}} \tag{3.23}$$

Now, using equations 3.20, 3.22, and 3.23, we will find that the effective transconductance is the same as that given in equation 3.21.

3.6 A CMOS Low Noise Amplifier

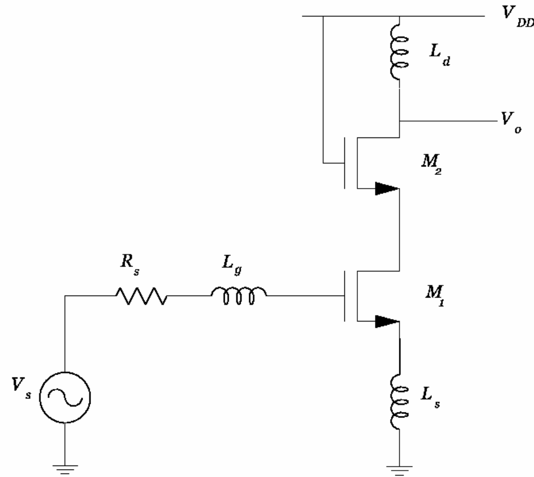


Figure 3.7. CMOS Low Noise Amplifier

Figure 3.7 shows a circuit that is commonly used in the design of CMOS low noise amplifiers. This circuit uses the input stage described in section 3.5 to provide an input match and current gain at the resonant frequency. A cascode is added to the input stage to mitigate the interaction between the input tank and output tank. The cascode also reduces the reverse gain through the amplifier, thus increasing the stability of the circuit. Furthermore, the cascode reduces the effect of the C_{gd} of M_1 by presenting a low impedance node at the drain of M_1. The output inductor, L_d, is designed to resonate at ω_o with the node capacitance at the output. The input and output tank can be aligned to provide a narrowband gain, but can also be offset from each other to provide a broader and flatter frequency response [24].

3.6.1 Voltage and Power Gain

Using equation 3.21, we can calculate the following expressions for the voltage and power gain assuming the LNA in figure 3.7 is input matched.

$$A_v = \left(\frac{\omega_t}{\omega_o}\right)\frac{R_L}{2R_S} \tag{3.24}$$

$$G_T = \frac{P_L}{P_{avs}} = \left(\frac{\omega_t}{\omega_o}\right)^2 \frac{R_L}{R_S} \tag{3.25}$$

where R_L is the resistance at the output due to the finite Q of L_d and the finite output resistance of the transistor.

3.6.1.1 Fundamental Limit of Gain

The gain of the amplifier shown in figure 3.7 can be improved upon by using an impedance matching network instead of inductive source degeneration, as shown in figure 3.8.

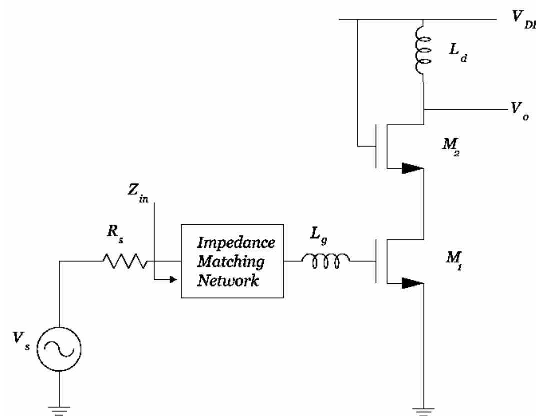


Figure 3.8. Input matching by using matching network

If the assumption is made that the matching network is lossless and can transform any impedance up to the source impedance, then the power available from the source is equal to

$$P_{avs} = \frac{\hat{v}_s^2}{8R_S} \tag{3.26}$$

The power available from the source will be transferred to the input of the transistor, where the following equation must hold:

$$\frac{\hat{v}_s^2}{8R_S} = \frac{\hat{v}_{gs}^2}{r_{g,NQS}} \tag{3.27}$$

From equation 3.27, it is observed that minimizing the real portion of the impedance at the input of the transistor results in more gain. Equation 3.27 presents the fundamental limit of gain because the non-quasi static gate resistance is always present and other parasitic resistances (i.e. due to layout) are not included. It is interesting to note that if the non-quasi static gate resistance is not included in the analysis, then one might arrive at the incorrect conclusion that there was no limit to gain since the input of the transistor is ideally capacitive, and no power can be dissipated in a purely reactive element [25].

3.6.2 Noise

To evaluate the noise performance of the circuit in 3.7, an equation for the noise factor will first be derived. The small signal noise model that will be used is shown in figure 3.9. It was shown in chapter 2 that the noise factor is the ratio between the total output noise power and the output noise power due to the source. Using equation 3.21, the total output noise power due to the source can be written as

$$P_{o,src} = P_{src} G_m^2 = \frac{4kT}{R_s(1+\frac{\omega_T L_s}{R_s})^2}(\frac{\omega_T}{\omega_o})^2 \tag{3.28}$$

The noise power at the output due to any series gate resistance can be found in a similar fashion as equation 3.28.

$$P_{o,R_g} = \frac{4kTR_g}{R_s^2(1+\frac{\omega_T L_s}{R_s})^2}\left(\frac{\omega_T}{\omega_o}\right)^2 \tag{3.29}$$

The channel thermal noise of the transistor appears at the output of the transistor, and has a output noise power equal to

$$P_{o,i_d} = \frac{4kT\gamma g_{d0}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{3.30}$$

To find the output noise power contribution of the gate noise, first re-write the gate noise as

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta g_g(1-|c|^2) + 4kT\delta g_g|c|^2 \tag{3.31}$$

where the first term represents the portion of the gate noise uncorrelated with the drain noise, and the second term represents the portion that is correlated with the drain noise. The contributions of the drain noise and the gate noise to the output power can be combined. The analysis is done in [26], and is repeated below.

$$P_{o,i_g+i_d} = \frac{4kT\gamma\chi g_{d0}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{3.32}$$

where

$$\chi = 1 + \frac{2|c|}{\omega_o R_s C_{gs}} \sqrt{\frac{\delta\alpha^2}{5\gamma} + \frac{\delta\alpha^2}{5\gamma}(1 + \frac{1}{(\omega_o R_S C_{gs})^2})} \qquad (3.33)$$

Finally, the noise factor of the low noise amplifier can be solved for using equations 3.28, 3.29, 3.30, 3.32. The noise factor is equal to

$$F = 1 + \frac{R_g}{R_s} + \frac{\gamma}{\alpha} \chi g_m R_s (\frac{\omega_o}{\omega_T})^2 \qquad (3.34)$$

The noise factor can be expressed in a more intuitive form if power/impedance matching is assumed at the input (which is often the case). The derivation is done in [27], and the result is repeated below:

$$F \approx 1 + \frac{\gamma}{\alpha} (\frac{\omega_o}{\omega_T})^2 (g_m R_s + \frac{2}{5}) + \frac{\alpha\delta (1 - |c|^2)}{5 g_m R_s} \qquad (3.35)$$

where the portion of the gate noise that is correlated with the drain noise has been neglected. In equation 3.35, the second term is the contribution from the channel drain noise, and the last term is the contribution from the uncorrelated portion of the gate noise. It can be observed that as ω_T increases with improving technology, the drain noise contribution will become less significant if the operating frequency is kept constant. The noise factor equation also shows that there is a minimum noise factor for a given ω_T since the drain noise is proportional to g_m, while the uncorrelated gate noise is inversely proportional to g_m. This implies that for a given current, there is a transistor size that corresponds to the minimum noise factor.

3.6.3 Linearity

An important metric of linearity in narrowband amplifier design is the input third order intermodulation point (IIP_3) of the circuit. The IIP_3 of the circuit in figure 3.7 can be written as [28]

$$IIP_3[dBm] = IIP_{3,in}[dBm] - 20\log_{10}\left(\frac{1}{\omega_o C_{gs} R_s}\right) \tag{3.36}$$

where an input match is assumed. The first term in equation 3.36 is the intrinsic IIP_3 of the device, and arises from the fact that short channel CMOS transistors exhibit velocity saturation, which gradually linearizes the ideal quadratic of the long channel drain current equation. The second term results from the extra voltage boost across the C_{gs} due to the series tank.

4

On-Chip Spiral Inductors

4.1 Introduction

Often times, the performance of an RF circuit is limited by the quality of the on-chip passive components, and in particular, on-chip inductors. Inductors are widely used in RF circuitry to resonate with capacitors and to provide impedance transformations. As a consequence, much research has been done to model them and improve upon their performance. This chapter will introduce the design and modeling of on-chip spiral inductors.

4.2 Spiral Inductors

A layout of a square spiral inductor is shown in figure 4.1. The parameters used to describe a spiral inductor are its number of turns (N), its outer length of a side (L), its line width (W), and its line spacing (S). Usually, the inductor is made on the top available metal layer so that the parasitic capacitance to the lossy substrate is minimized, while the underpass is made in the next highest metal layer. The inductor is separated from the substrate by layers of inter-layer dielectric. It is possible to decrease the series resistance

by using a circular or octagonal spiral instead of a square. However, non-Manhattan geometries are not supported by some layout tools. [29]

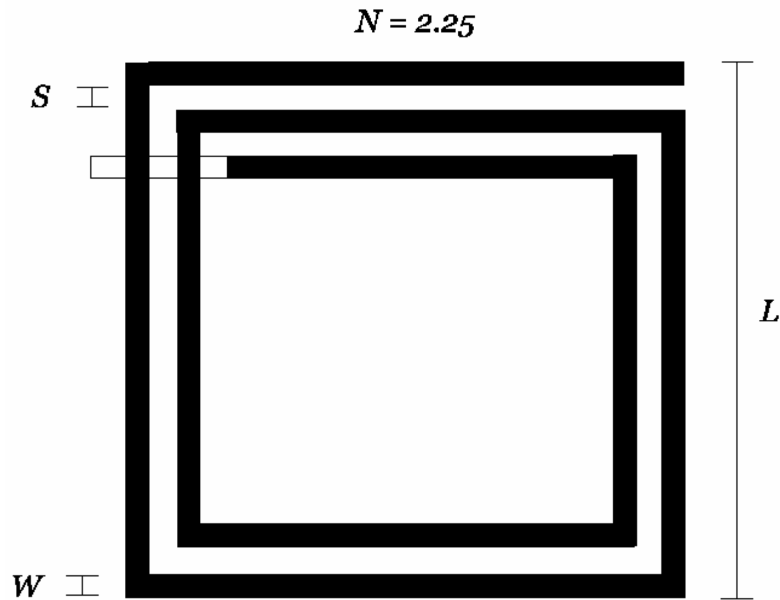


Figure 4.1. Layout of a spiral inductor

4.3 Losses in Spiral Inductors

An ideal inductor is able to store electrical energy in its coils without dissipating any of it in the process. However, practical inductors have loss mechanisms that convert electrical energy to other forms of energy (such as heat) that cannot be recovered. In this section, some loss mechanisms will be summarized.

4.3.1 Resistive Losses and Eddy Currents

In standard CMOS processes, metal lines are made with aluminum or copper, which have finite conductivity. As a result, resistive losses will occur in the inductor, and a resistor in series with the inductor models this loss. Using multiple metal layers in parallel to create a shunt inductor can mitigate this loss mechanism.

Besides the finite conductivity of the metal, there are eddy currents in the conductor that result from the skin and proximity effects that oppose the current flow.

Eddy currents cause the series resistance to increase with increasing frequency. The series resistance will increase due to the fact that current flow will move towards the outer areas of the conductor, which decreases the effective cross-sectional area, and causes an increase in current density. The reason that the currents tend to migrate toward the outer portion of the conductor is because magnetic fields penetrate the volume of the conductor, causing electric fields to be produced there [30]. Thus, the impedance within the conductor is increased, and current flow becomes more restricted towards the outer portion of the conductor. The skin effect results from the self-inductance of the conductor and can be quantified by the effective depth of penetration, also known as the skin depth:

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{4.1}$$

where ω is the frequency, μ is the permeability, and σ is the conductivity.

Whereas the skin effect results from the self-inductance of the conductor, the proximity effect is due to the mutual inductance of other nearby conductors. In spiral inductors, nearby conductors increase the magnetic field, causing an increase in the series resistance.

4.3.2 Substrate Losses

Ideally, RF designers would like the substrate to have a high resistivity so that the loss through it is minimized. However, most modern CMOS processes use a conductive substrate to minimize the possibility of latch-up [31]. While this is desirable for digital designers, it is a problem for RF designers because the conductive substrate causes electromagnetic energy to be radiated as heat in the substrate. One loss mechanism is the displacement current that flows perpendicular to the spiral segments through the substrate to nearby grounds. This current is induced by the electric field. Eddy currents are also present in the substrate as a result of the time-varying magnetic fields that penetrate the

substrate. As opposed to displacement current, eddy currents in the substrate flow parallel to the spiral segments.

4.4 Inductor Figures of Merit

In this section, three common figures of merit used to describe the characteristics of an inductor are introduced. They are the inductance, quality factor, and self-resonant frequency.

4.4.1 Inductance

The calculation of the inductance of a structure is based upon Grover's formulas for the self-inductance of a conductor, and the mutual inductance between two conductors. Using Grover's formulas, Greenhouse devised a formula to solve for the total inductance of a spiral structure [32]. It states that the total inductance of a spiral structure is equal to the sum of all of the self-inductances of the wire segments and the positive and negative mutual inductances between the wire segments. Two segments have a positive mutual inductance if the direction of current flow is the same, and a negative mutual inductance if the direction of current flow opposes each other. In the case of a spiral inductor, the segments on the same side have positive mutual inductance, while segments on opposite sides have negative mutual inductance. For a spiral inductor, there are 4N self-inductance terms, 2N(N-1) positive mutual inductance terms, and $2N^2$ negative mutual inductance terms, where N represents the number of turns. Often times, the calculation gets prohibitively complicated, and is best solved by a computer simulation program like ASITIC [33] or HFSS (full EM solver).

4.4.2 Quality Factor

The quality factor is defined as

$$Q = 2\pi \frac{Energy \quad stored}{Energy \quad dissipated} \tag{4.2}$$

and is a measure of the amount of loss in a device. An ideal inductor has a Q of infinity. Applying this definition to an ideal inductor in series with a resistor results in the following equation:

$$Q = \frac{\omega L}{R} \tag{4.3}$$

4.4.3 Self-Resonant Frequency

The self-resonant frequency is the frequency at which the inductor will resonate with its own parasitic capacitance. Below the self-resonant frequency, the inductor behaves like an inductor, at the self-resonant frequency the inductor behaves like a resistor, and above the self-resonant frequency, the inductor behaves like a capacitor in the absence of load capacitance. However, in general there is load capacitance present, and the frequency of operation of the inductor is usually below its self-resonant frequency.

4.5 Inductor Modeling

In the design of RF circuits, an accurate inductor model is of great importance. In this section, a simple narrowband model that is useful for circuit analysis is presented. However, before the parameters of the model can be extracted, the raw S parameters from the network analyzer must be de-embedded in order to obtain accurate results.

4.5.1 De-embedding

De-embedding of the raw S parameters from the network analyzer is necessary because typically there are parasitics not associated with the device under test (DUT) that are present due to the test setup. For example, test inductors have pads that are present only

for testing purposes. In general, it is necessary to also fabricate an open and a short along with the DUT. An open consists of only the pads used to test the DUT, and is used to remove the capacitance associated with the pads. The short consists of both the input and output connected to ground, and is used to remove any series inductance and resistance of the ground path, which is not associated with the DUT. A methodology for de-embedding the raw S parameters is shown in figure 4.2.

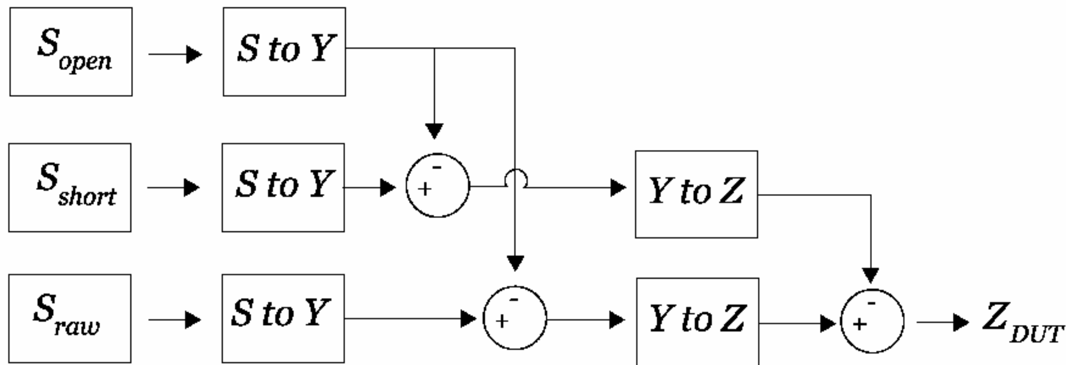


Figure 4.2. Flow for de-embedding raw S parameters

The various S parameters measured are converted to Y parameters so that the open can be subtracted since the pad capacitance is in parallel. Then, the results are converted to Z parameters so that the series resistance and inductance can be taken out. The final result is the Z parameter of only the DUT. It should be mentioned that the above methodology does not include the calibration of the measurement device itself. In general, that is done with the SOLT (short-open-load-through) method.

4.5.2 The Pi Model

The Pi model, shown in figure 4.3, is useful in RF circuit design because it can be solved easily given the S (and therefore Y) parameters at a single frequency. Its limitation is that it is a narrowband model, and might not be accurate over a wide range of frequencies. However, in many applications, the Pi model is accurate enough to be used.

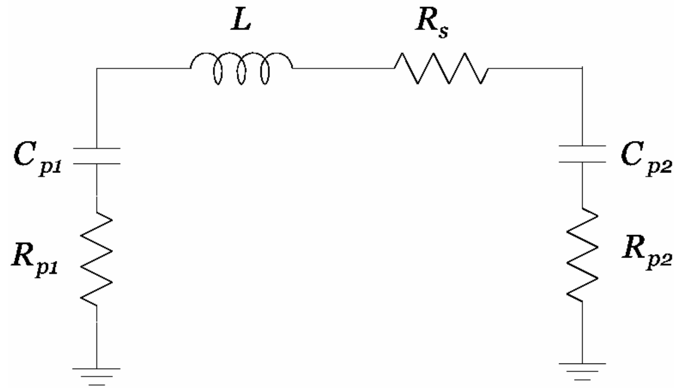


Figure 4.3. Pi model for modeling an inductor

Using the definitions for Y parameters from chapter 2, the circuit parameters can be solved for in terms of the measured (and de-embedded) Y parameters. The Y matrix is equal to:

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_1 + Y_2 & -Y_2 \\ -Y_2 & Y_2 + Y_3 \end{bmatrix} \tag{4.4}$$

where

$$Y_1 = \frac{j\omega C_{p1}}{1 + j\omega R_{p1} C_{p1}} \tag{4.5}$$

$$Y_2 = \frac{1}{j\omega L + R_s} \tag{4.6}$$

$$Y_2 = \frac{j\omega C_{p2}}{1 + j\omega R_{p2} C_2} \tag{4.7}$$

Before solving for the circuit parameters in terms of the Y parameters, it is useful to first define the quality factors of the inductor and capacitor as

$$Q_L = \frac{IM(Y_{12})}{RE(Y_{12})} \tag{4.8}$$

$$Q_{C1} = \frac{IM(Y_{11} + Y_{12})}{RE(Y_{11} + Y_{12})} \tag{4.9}$$

where Q_{C2} is equal to equation 4.9 with Y_{11} replaced by Y_{22}.

Using equations 4.5 – 4.9, the circuit parameters can be solved for, and are equal to

$$L = \frac{Q_L^2}{\omega}\left[\frac{1}{IM(Y_{12})(1 + Q_L^2)}\right] \tag{4.10}$$

$$R_s = -\frac{1}{RE(Y_{12})(1 + Q_L^2)} \tag{4.11}$$

$$C_{p1} = \frac{IM(Y_{11} + Y_{12})}{\omega}(1 + \frac{1}{Q_{c1}^2}) \tag{4.12}$$

$$R_{p1} = \frac{1}{RE(Y_{11} + Y_{12})(1 + Q_{c1}^2)} \tag{4.13}$$

C_{p2} and R_{p2} are equal to equations 4.12 and 4.13 with Y_{11} and Q_{c1} replaced by Y_{22} and Q_{c2}.

5

CMOS LNA Design

5.1 Introduction

The previous chapters have been focused on LNA fundamentals. In this chapter, the ideas introduced previously will be used in the design of a low power CMOS LNA. The design steps will first be described, followed by a brief discussion of the difficulties arising from low power deep submicron CMOS design. Finally, simulation results and the layout will be shown.

5.2 A Low Power CMOS LNA

The most important requirement for the transciever in the PicoRadio project is that it must be low power such that its energy can be scavenged from the environment. As a consequence, the low noise amplifier must be optimized at the lowest power possible. The limiting requirement for the low noise amplifier is the gain, so this leads to the current-reuse architecture shown in figure 5.1. The following sections detail the design steps for the current-reuse low noise amplifier.

5.2.1 Current-Reuse Topology

The idea behind current-reuse ("stacked") topologies is to recycle the bias current so that it can be used by more than one stage. Figure 5.1 illustrates a current-reuse LNA topology that combines the inductive source degeneration architecture with a common source amplifying stage [34] [35]. The signal is coupled through a capacitor from the drain of the first stage to the gate of the second. The capacitor at the drain of the second stage is made large so that it serves as an AC ground. A potential problem with this topology is that headroom and output swing is now an issue since two stages are now stacked on top of each other. Also, the parasitic bottom plate capacitance of the coupling capacitor could limit the gain [36].

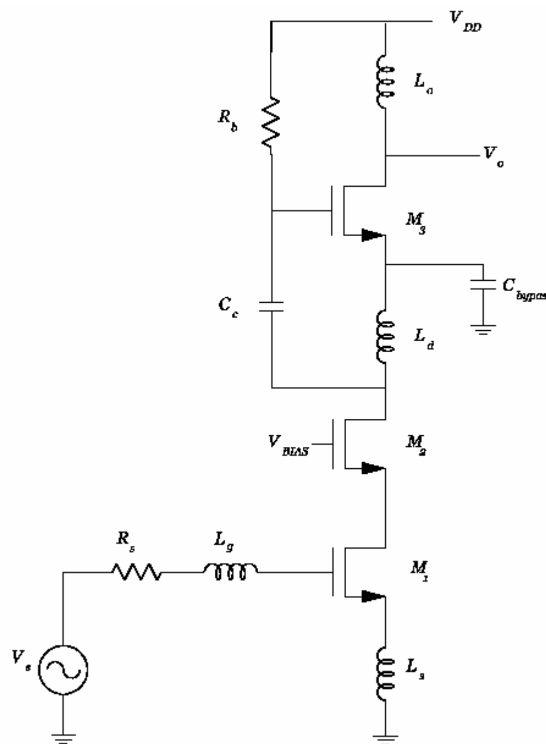


Figure 5.1. Current – reuse LNA topology

5.2.2 Importance of Input Parasitic Capacitance

An important parasitic capacitance to take into account when using the architecture of figure 5.1 is the input parasitic capacitance C_p, as shown in figure 5.2. This capacitance becomes significantly important when designing for low power in deep submicron CMOS. The combination of those two factors tend to make the device size of the input transistor small. This in turn makes the C_{gs} small, which makes the effect of C_p non-negligible. This parasitic capacitance results from the ESD protection diodes, the bonding pad, the capacitive coupling from the board, and the gate to drain capacitance from the input device itself. In the following sections, the effect of this parasitic capacitance on the resonant frequency and gain will be examined.

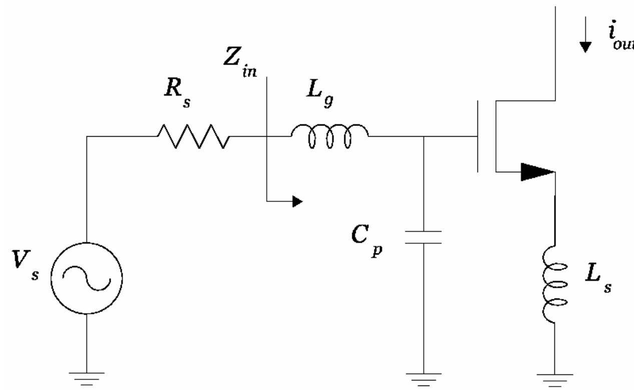


Figure 5.2. LNA with parasitic capacitance at input

5.2.2.1 Effect of C_p on Input Matching

Previously, equation 3.16 showed the values of the parameters that were necessary to achieve an input match, and equation 3.17 gave the frequency at which this occurred. However, if C_p is considered, then the input impedance at ω_o is now given by

$$Z_{in}(\omega_o) \approx \frac{g_m L_s}{C_{gs} + C_p} + r_{g,NQS} \frac{C_{gs}}{C_{gs} + C_p} - \frac{g_m \omega_o^2 L_s L_g C_p}{C_{gs} + C_p} \quad (5.1)$$

where ω_o is now equal to

$$\omega_o \approx \frac{1}{\sqrt{(L_s + L_g)C_{gs} + L_g C_p}} \tag{5.2}$$

From equation 3.37, it can be seen that the effect of C_p is to reduce the input impedance of the LNA. As a consequence, for a fixed device, L_s will have to be increased from the ideal value initially calculated in equation 3.16. Increasing L_s will decrease the gain due to the input tank being de-Qed.

5.2.2.2 Effect of C_p on G_m

To examine the effect of C_p on gain (voltage or power), one can look at the overall transconductance of the circuit. The G_m of the circuit shown in figure 5.2 is

$$G_m \approx \left(\frac{\omega_t}{\omega_{o,g}}\right)\frac{1}{R_S(1+\frac{C_p}{C_{gs}})+(\frac{g_m L_s}{C_{gs}}+r_g)(1-\omega_{o,g}{}^2 C_p L_g)} \tag{5.3}$$

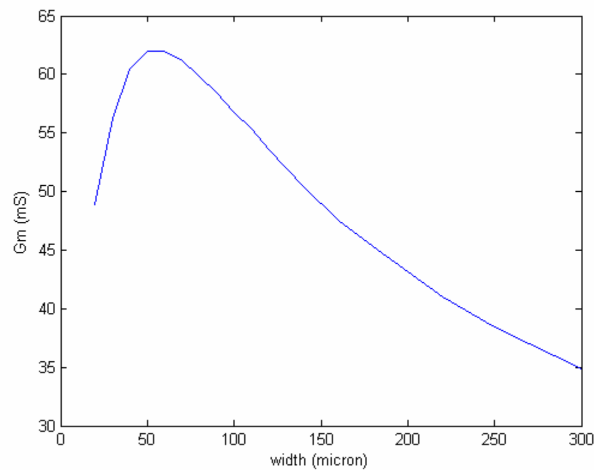
where $\omega_{o,g}$ is the frequency at which the maximum gain occurs, and is equal to

$$\omega_{o,g} \approx \frac{1}{\sqrt{(L_s + L_g)C_{gs} + L_g C_p + g_m L_s C_p R_s}} \tag{5.4}$$

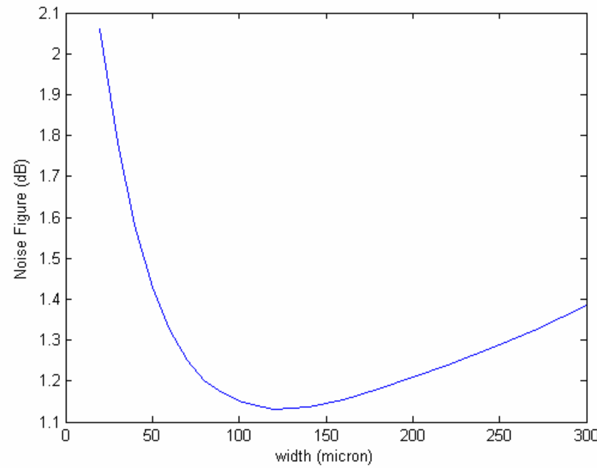
It is interesting to note that the frequency for input match and maximum G_m were the same in the ideal case, but the addition of C_p has made the frequency for maximum G_m (equation 5.4) lower than that for an input match (equation 5.2). Therefore, a perfect input match and maximum gain cannot be achieved simultaneously.

5.2.3 Sizing the First Stage

The sizing of the input device is of utmost importance since it has the greatest impact on the LNA figures of merit. In this optimization procedure, an inductively degenerated common source input stage similar to the one shown in figure 3.7 was used. Figures 5.3a and 5.3b are plots of the transconductance of the LNA and the noise figure of the LNA with respect to the width of the input device. The plots were generated under the restriction that the resonant frequency of the device has to equal 1.9 GHz, and that there must be an input match at this frequency. In this design, the gate inductor is off chip, so the parasitic capacitance of the bonding pad was included. It should also be noted that the transistor model that was used does not include the NQS resistor in the AC analysis, so an explicit resistor with value equal to that given in equation 3.5 was added in series with the gate.



(a)



(b)

Figure 5.3. Optimization plot of input device width versus (a) G_m (b) Noise Figure

The two plots above confirm what one might suspect from the equations presented in chapter 3. The plots were generated by varying the width of the input device while keeping the resonant frequency and bias current constant. Furthermore, an input impedance match was maintained, according to equation 5.1 and at the resonant frequency given by equation 5.2. The first plot shows that the overall transconductance of the input stage is proportional to f_T. For small widths, the parasitic capacitance at the input is dominant, which results in lower f_T. This is due to the fact that the parasitic capacitance remains constant while g_m is decreasing with decreasing width. Conversely, f_t will also increase with increasing width when the parasitic capacitance at the input is dominant compared to C_{gs}. Once the gate to source capacitance of the device becomes dominant, f_T becomes independent of width. For large widths, the device goes into velocity saturation, which causes f_T to decrease.

The second plot can be interpreted as follows. For small device widths the g_m of the device is small, so the NQS gate noise dominates the noise figure since the noise is inversely proportional to g_m. For large device widths, the device's drain noise will dominate the noise figure. Fundamentally, this trade-off exists because the gain of the device is not proportional to g_m, while the NQS gate noise is inversely proportional to g_m, and the channel drain noise is proportional to g_m. This fact also leads to the observation

that an increased f_t not only increases the gain of the device, it reduces the noise figure as well. Finally, it is worth mentioning that it is useful and desirable to use the minimum length for the input device in order to maximize the f_t since f_t is a function of the transit time.

It should be noted that without C_p and for a given bias current, f_t will continue to increase as the width decreases. This is because ($V_{gs} - V_t$) continues to increase, and f_t will continue to increase until the device goes into the triode region. In the CMOS process and bias current that was used, this resulted in very small (and unreasonable) device widths. Therefore, the decrease in g_m for the device widths that are shown in figure 5.3a is solely due to the presence of C_p.

5.2.4 Sizing the Second Stage

The purpose of the second stage of the low noise amplifier is to further increase the gain. However, since the second stage is not cascoded, the isolation between the output and input might not be high enough. Therefore, care must be taken to keep the C_{gd} of the device small. Increasing the length of the transistor also helps to improve the isolation as well. Furthermore, the C_{gs} of the device and the coupling capacitor cause a capacitive divider between the output of the first stage and the input of the second stage. The C_{gs} of the device was made much smaller than the coupling capacitor in order not to degrade gain. The size of the transistor was adjusted through simulation until the gain and isolation were satisfactory.

5.2.5 Inductor Design

The inductors that need to be designed for this LNA are the ones at the gate and source of the input device, and at the output of the first and second stages.

It was decided that the gate inductor should be placed off-chip because the inductance was too big to be placed on-chip, and the low values of Q achievable in CMOS processes would degrade both the noise figure and gain. However, the parasitic capacitance of the bonding pad at the input must now be taken into account. To deal with

the bonding pad capacitance, some designs [37] [38] shield the pad with a metal tied to the source of the device. However, this strategy directly degrades the f_t of the device. In this work, the pad was shielded with a metal that was tied to ground.

The source inductor was designed assuming a parasitic input pad capacitance and by using the equations for an input impedance match introduced earlier in this chapter. The source inductor was put on-chip, and was designed using a ST Microelectronics inductor p-cell. In order to increase the Q, the inductor is made on metal 6 and metal 5 connected in parallel.

In order to achieve high gain, it is necessary to have a large high Q inductor at both the outputs tanks of the first and second stages since the load impedance at resonance is equal to

$$R_L \approx \omega_o LQ \tag{5.1}$$

However, there is a limitation on the maximum inductance possible since too large an inductance would cause too low of a self-resonant frequency. Furthermore, too high a Q value would make it difficult to line up the tanks since the bandwidth is equal to

$$BW \approx \frac{\omega_o}{Q} \tag{5.2}$$

Taking these considerations into account, a shunt inductor on metal 6 and metal 5 was created using the ST Microelectronics inductor p-cell framework.

Obtaining an accurate model for simulation was necessary in order to insure good results. A 3-dimensional electromagnetic field solver was used (HFSS) to obtain the S parameters. From these results, a PI model was constructed using the values at 1.9 GHz. To verify the accuracy at other frequencies, the inductor PI model was simulated and the S-parameters compared with that from HFSS. The PI model showed good results at the frequencies of interest (~500 MHz – 2.5 GHz). The PI model was then used in the simulation of the LNA.

5.2.6 Output Impedance Matching Network

In order to interface the LNA with the test equipment the output impedance much be transformed down to 50 ohms. To accomplish this, the capacitive divider shown in figure 5.4 was used. [39]

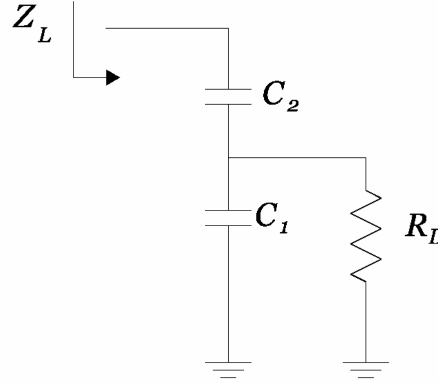


Figure 5.4. Capacitive divider as an impedance transformer

The impedance Z_L is now equal to

$$Z_L = \frac{1 + [\omega_o R_L (C_1 + C_2)]^2}{\omega_o^2 R_L C_2^2} \tag{5.3}$$

and the equivalent capacitance that the transformer presents to the output load is

$$C_{eq} = \frac{C_2 + \omega_o^2 R_L^2 C_1 (C_1 + C_2) C_2}{1 + [\omega_o R_L (C_1 + C_2)]^2} \tag{5.4}$$

If $[\omega_o R_L (C_1+C_2)]^2 >> 1$ then equations 5.3 and 5.4 simplify to

$$Z_L \approx R_L \left(\frac{C_1 + C_2}{C_2} \right)^2 \tag{5.5}$$

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \tag{5.6}$$

The capacitive impedance matching network must transform the load impedance such that it equals the output impedance of the LNA. The other requirement is that it the equivalent capacitance seen at the output tank must resonant with the output inductor at the resonant frequency.

In order for good matching, the capacitors must be accurate and have very little parasitic bottom plate capacitance. In this design, MIM capacitors were used.

5.3 Difficulties in Low Power Design

While it seems attractive that improved process technology (increased f_t) will result in higher gain, system-level integration considerations complicate the design. The problem results from the fact that increases in f_t will result in large values of L_g and very small values of L_s, both of which can pose problems. The small value of L_s is problematic because it is sensitive to parasitic inductances, reducing the accuracy of the input match impedance. The large value of L_g,, whose size is determined by the operating frequency, makes it difficult to implement on-chip in modern CMOS processes while still maintaining a high quality factor. Using an off-chip inductor also introduces a parasitic capacitance at the input, which alters the resonant frequency and decreases the G_m. When biasing low current RF amplifiers to operate with a maximum f_t, it is essential to include the effect of this capacitance since in modern processes it is on the same order of magnitude as C_{gs}. Increasing the bias current allows for larger device widths for the same f_t, which makes the design less sensitive to parasitics, as well as facilitating integration.

5.4 Simulation Results

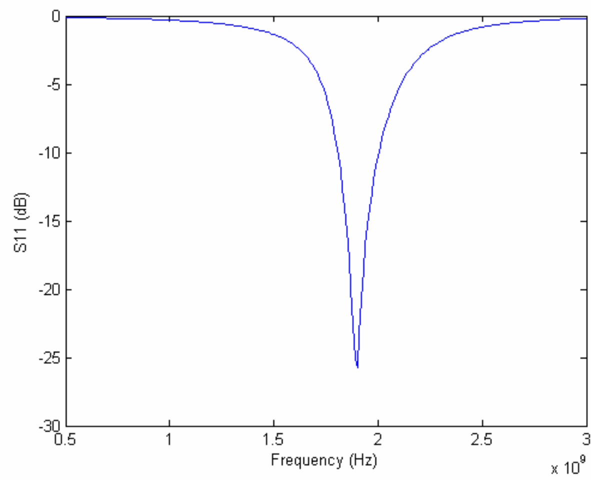
The design was simulated using the BSIM3 models provided for the ST Microelectronics 0.13 μm CMOS process. The on-chip inductors were modeled using results obtained

from a 3D electromagnetic field solver, and the off-chip inductor was modeled using a circuit model obtained from the manufacturer. Important parasitic capacitances such as bottom plate capacitance and pad capacitance was included in the model. Since the model does not incorporate the non-quasi static gate resistance, a resistor with value equal to that of equation 3.5 was added in series with the gate. However, by adding only a resistor, the non-quasi static gate noise will be underestimated since δ is greater than 1. The noise figure was simulated using a matched load. Table 5.1 summarizes the performance of the LNA, and the following sections show simulation plots.

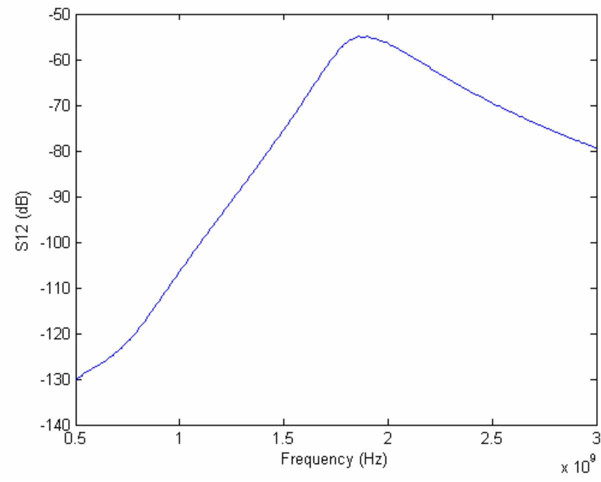
Parameter	Value
Frequency	1.9 GHz
Bias Current	936 μA
Power Supply Voltage	1.2 V
S_{11}	-25.7 dB
S_{12}	-54.9 dB
S_{21}	29.1 dB
S_{22}	-12.05 dB
A_V (unloaded)	37.84 dB
Noise Figure	1.85 dB
IIP3	-20.2 dBm

Table 5.1. Summary of LNA performance parameters

5.4.1 S Parameters



(a)



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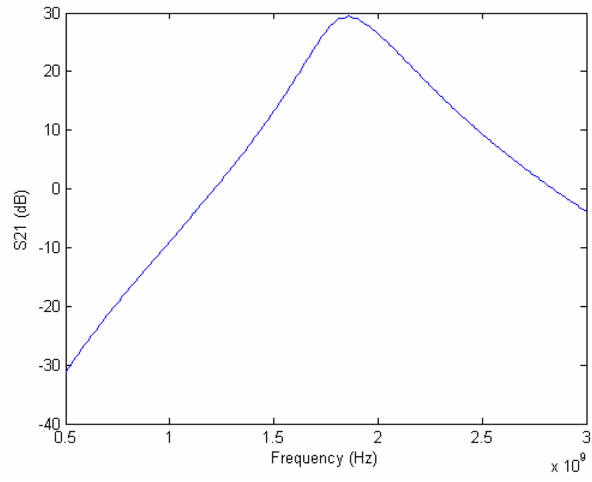

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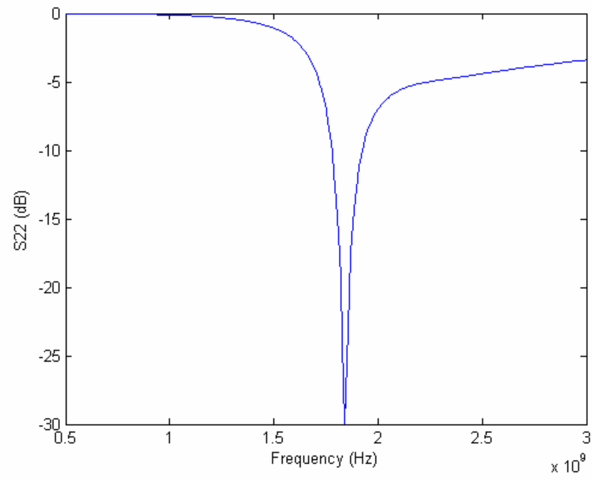
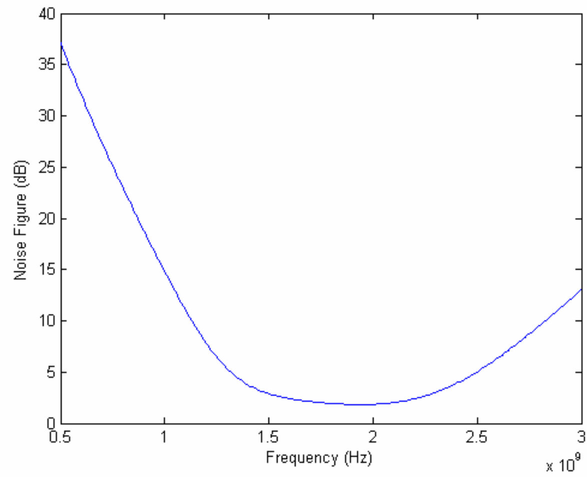


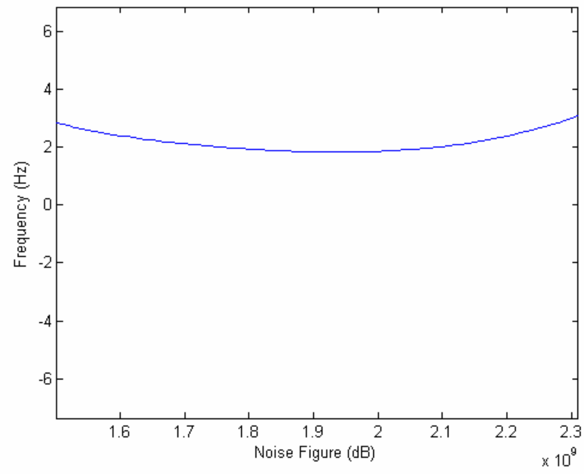
(d)

Figure 5.5. Plots of (a) S_{11} (b) S_{12} (c) S_{21} (d) S_{22}

5.4.2 Noise Figure



(a)



(b)

Figure 5.6. (a) Noise figure (b) Zoom in to minimum

5.4.3 Voltage Gain

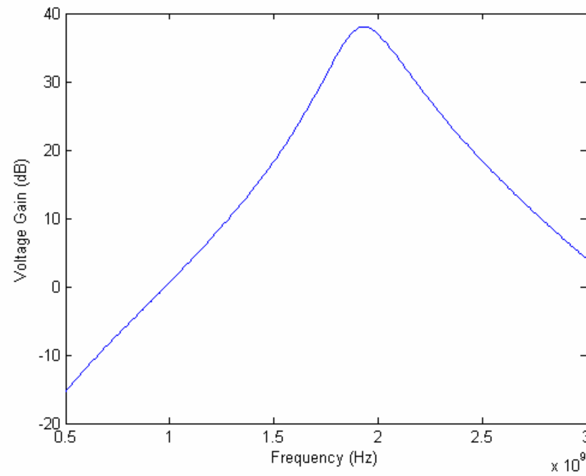


Figure 5.7. Unloaded voltage gain

5.4.4 Layout

It was stated before that reducing parasitics is absolutely necessary in order to achieve good performance. One way to reduce parasitics is though good layout. One important parasitic capacitance mentioned previously is C_p. In order to reduce this capacitance, the smallest pad was used, and a small diode was placed at the input node for ESD protection. Furthermore, the signal line was made on the highest metal, and care was taken not to make the line too thick. Another important capacitance that must be minimized is the bottom plate capacitance. In order to minimize this capacitance, MIM capacitors were used. To reduce the interaction of the inductors with each other and other parts of the circuit, they were placed away from each other and the rest of the circuit in the layout. To reduce the interaction between the signal lines, ground pads were placed on both sides of the input and output pads. Furthermore, it is necessary to reduce the interaction between the input and output signal lines. Too much interaction between these lines would cause positive feedback between the input and output, which in turn could cause the LNA to oscillate. To reduce the amount of

coupling, the input and output signal lines were placed a safe distance apart. One final note about the layout is that bypass capacitors were placed on all bias lines in order to reduce their noise contributions.

Figure 5.8 shows the layout of the current-reuse LNA.

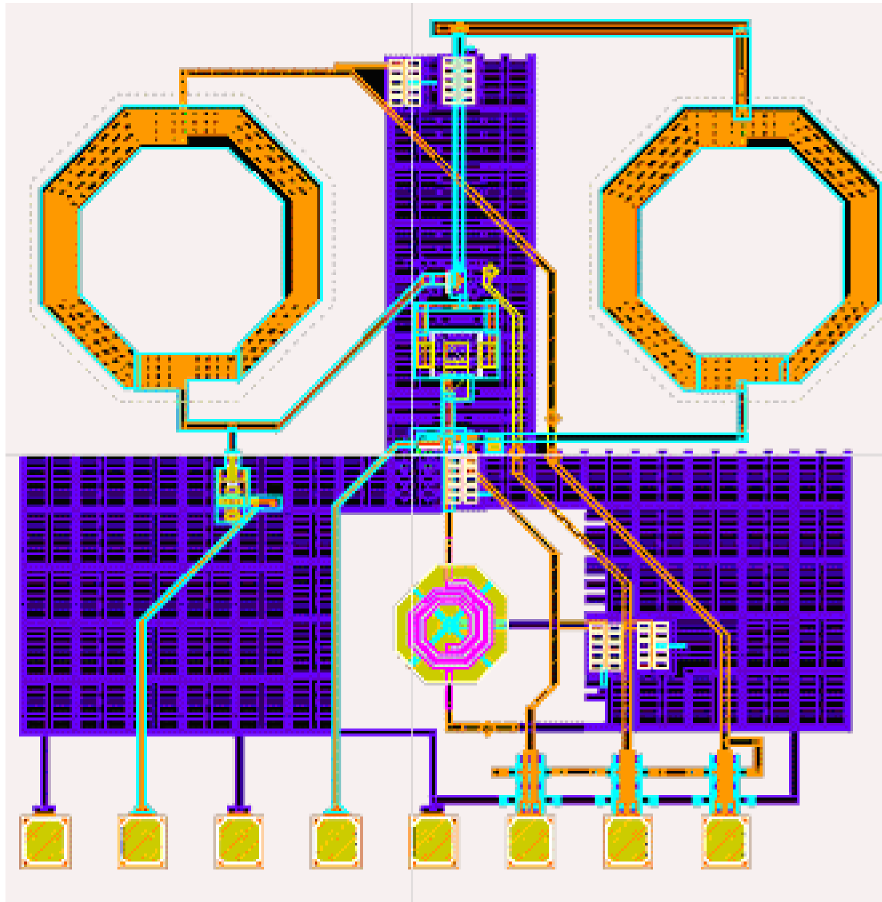


Figure 5.8. Layout of current-reuse LNA

The current-reuse LNA described in this chapter has been sent out for fabrication in the ST 0.13 μm process.

6

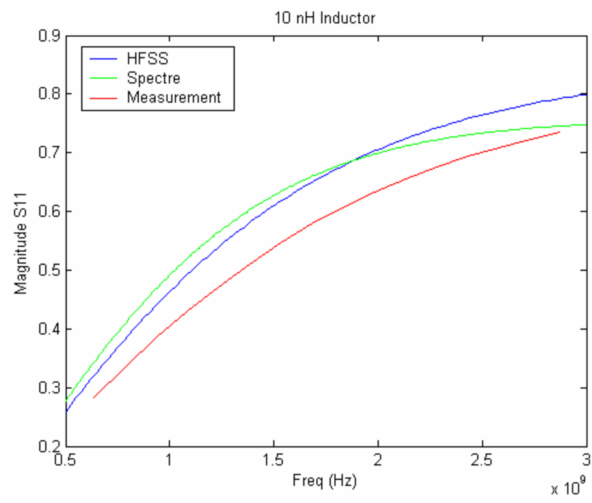
Results

6.1 Introduction

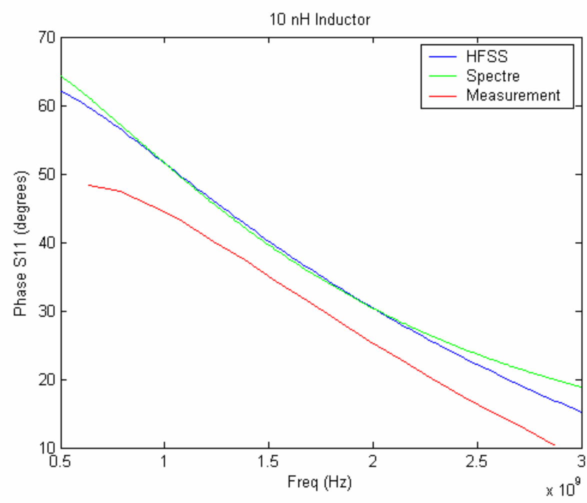
To help characterize the current-reuse LNA described in chapter 5, a prototype first stage LNA and a test structure for the output inductor was fabricated and tested. This chapter presents the experimental results obtained from the measurements.

6.2 10 nH Inductor

Proper characterization of the output inductor is critical in the design of the LNA because the output inductor determines the resonant frequency of the output tank, the gain of the LNA, and the output impedance. Therefore, characterization of the output inductor by experimental measurements, and comparison to the simulation model is necessary in order to insure accurate design. The S parameter plots shown in figure 6.1a-d confirm good agreement between simulation and measurement at frequencies around 1.9 GHz. The measurement curve is just a plot of measurement data. The HFSS curve is a plot of the simulated S parameters from HFSS. The Spectre curve is a plot of the simulated S parameters using an extracted PI circuit model with L = 10.4 nH, R_s = 3.78 Ω, R_{p1} = R_{p2} = 307.7 Ω, C_{p1} = C_{p2} = 181.6 pF.



(a)



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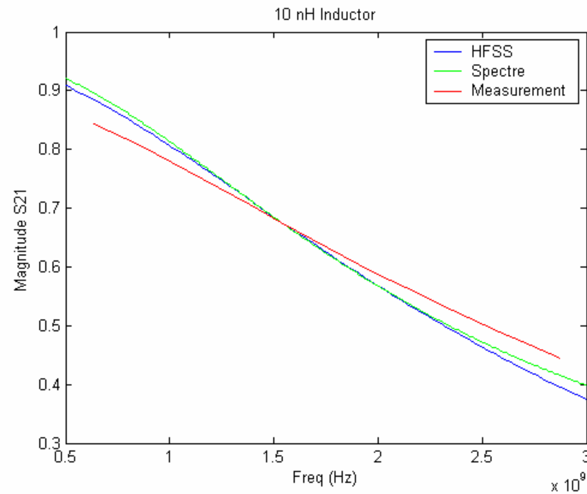

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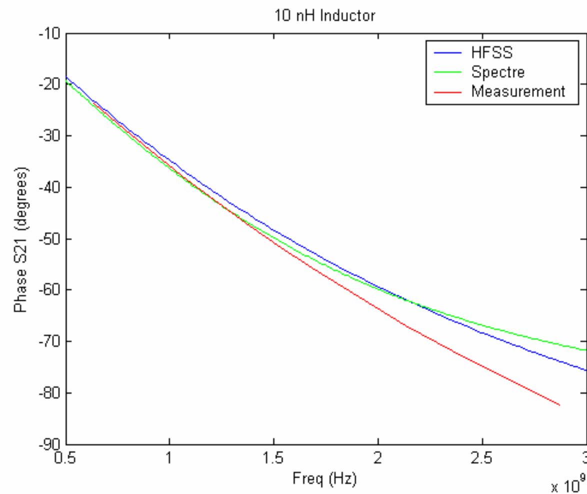

(d)

Figure 6.1. Comparison of results for (a) magnitude S_{11} (b) phase S_{11} (c) magnitude S_{21} (d) phase S_{21}

6.3 Prototype LNA

Besides the output inductor, it is also important to have an accurate characterization of the first stage of the LNA. The LNA circuit shown in figure 3.8 was designed, fabricated and measured. This prototype LNA is exactly the same as the first stage of the current-reuse LNA designed in chapter 5 except for the input impedance matching. In the prototype, the impedance matching is done with an off chip matching network instead of

with inductive source degeneration. Figure 6.2 below is a plot of the measured S parameters of the LNA.

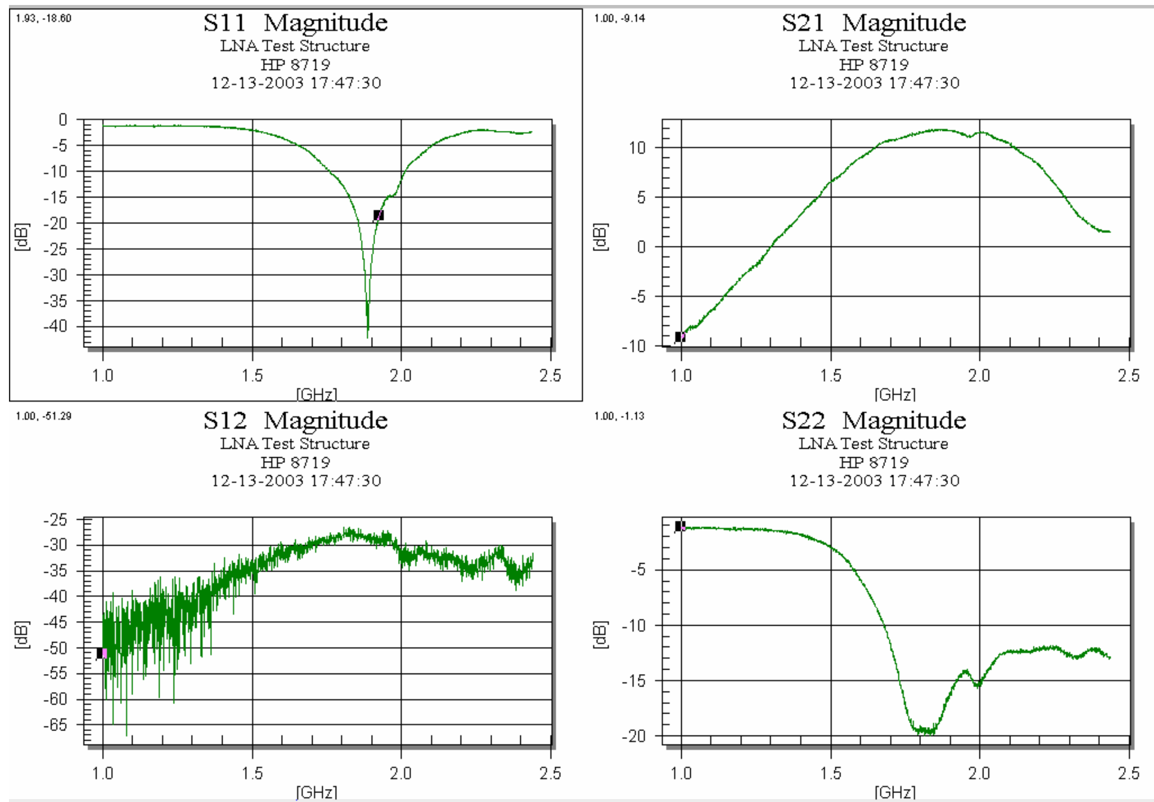

Figure 6.2. Experimental S parameter measurement plots

The LNA was initially designed without the addition of parasitic board capacitance because it was thought that a hole cut in the ground plane underneath the board trace would be sufficient in reducing this capacitance. However, this was not the case, and an estimated 1 pF of parasitic board capacitance is present at the sensitive LNA input node. As a result of this capacitance, the LNA gate inductor had to be changed manually from 16 nH to 6 nH. In the process of manually changing the gate inductor however, some of the gates of the input device were blown (the input device is made up of 45 smaller devices in parallel). This hypothesis is supported by the fact that a DC bias voltage exists at the gate of the input device when the supply voltage is turned on but the gate bias voltage has not been. The DC bias points were measured before the manual changing of the gate inductor, and this effect was not present. Nevertheless, the LNA was biased up

to the proper bias current and measurements were taken. The results are to be worse than expected initially due to the partially blown gates of the input device. All data were obtained at V_{DD} = 1.2 V and I_{BIAS} = 1.5 mA.

Parameter	Measurement
Magnitude S_{11}	-28 dB
Magnitude S_{12}	-29 dB
Magnitude S_{21}	11.6 dB
Magnitude S_{22}	-17 dB

Table 6.1. Experimental S parameter measurements

At the time of this writing, only the S parameters are available. Linearity and noise figure measurements are currently being performed.

7

Conclusions

In this work, the design, simulation, and layout of a 1 mW 0.13 μm CMOS low noise amplifier with 29 dB of power gain and a noise figure of 1.85 dB was shown. In an effort to obtain a more accurate design of the LNA, individual blocks were first characterized with experimental measurements. It was shown that the PI circuit model used for the output inductor achieved accurate results. This statement is further strengthened by the measured S_{22} of -17 dB of the prototype LNA. The first gain stage of the LNA was also measured, and it was learned that the parasitic board capacitance at the input node was about 1 pF more than expected. This will cause shift in the resonant frequency which must be compensated by changing the gate inductor. In the manual changing of the gate inductor during testing, it was observed that the gate of the input transistor was partially blown, which caused a decrease in the forward gain. Nevertheless, the LNA was still able to produce a S_{11} of -28 dB as well as a S_{21} of 11.6 dB.

From this work, many conclusions about low power RF amplifier design can be made. It was shown that a current-reuse topology could be implemented to save power and achieve high gain and good noise figure at the cost of output swing. It was also shown that in low power, deep sub-micron design, the parasitic capacitance of the bonding pad at the input node of the LNA cannot be ignored, and causes a shift in the resonant frequency and affects both the gain and input matching. Another conclusion

that can be made is that advancements in CMOS technology theoretically improves both the gain and noise figure of the LNA. However, the quality of on-chip passives, and parasitic capacitances and resistances from the board, pads, and layout makes the realization difficult. Furthermore, the small device sizes of the transistors in low power, deep sub-micron technology designs make integration of passives, specifically inductors, increasingly difficult. This problem is further compounded by the fact that off-chip components introduce parasitics from the board and the bond wires. These parasitics cannot be ignored and must be modeled in simulation in order to achieve good results.

There is much work to be done in the area of low power, deep sub-micron CMOS LNA design. The improvement in technology has given designers a chance to capitalize upon the increased gain and reduced noise figure that is possible. The issue of integration of passives is also an area that can be improved upon. This design space is indeed different from conventional LNA design spaces, and is open to a whole world of possibilities.

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