

30 GHz CMOS Low Noise Amplifier

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Abstract—A 30 GHz low noise amplifier was designed and fabricated in a 90nm digital CMOS process. The mm-wave amplifier has a peak gain of 20 dB at 28.5 GHz and a 3dB bandwidth of 2.6 GHz with the input and output matching better than 12 dB and 17 dB over the entire band respectively. The NF is 2.9 dB at 28 GHz and less than 4.2 dB across the band and it can deliver 2 dBm of power to a matched load at its 1 dB compression point. The amplifier has a measured linearity of IIP3=-7.5 dBm. It consumes 16.25 mW of power using a low supply voltage of 1 V and occupies an area (excluding the pads) of $1600\mu\text{m} \times 420\mu\text{m}$

Index Terms—CMOS mm-wave Amplifier, CMOS Low Noise Amplifier (LNA), Round-Table Transistor.

I. INTRODUCTION

In the past mm-wave circuits were fabricated with high performance and expensive III/V technologies because of their better electron mobility, higher breakdown voltage and nearly insulating substrate. With today's scaled down CMOS transistors having f_t and f_{max} exceeding 100 GHz, operating at tens of gigahertz frequency range with relatively inexpensive and highly integrable standard CMOS process is possible [1]- [9]. In this paper we demonstrate an LNA operating at 30 GHz with performance comparable or better than amplifiers designed in other more advanced technologies.

There are some major disadvantages in employing a digital CMOS process at mm-wave frequency range. Transistors have lower available gain at the desired band so there is less room for modeling errors and mismatches. Moreover the conductive substrate adds parasitic losses which complicates the active and passive device modeling. Metal layers are relatively thin and in close proximity to the conductive substrate. Compared to insulating substrates, quality factors for matching elements, interconnects, and resonators are lower. Furthermore the proximity to the substrate increases the capacitive coupling and lowers the self resonance frequency of passive devices.

Since we are operating at the frequency limits of the transistors, careful design requires incorporation of losses and parasitic effects in active and passive devices. This requires a dual approach to design which includes device and layout optimization besides circuit design. In section II we discuss component design and methods to achieve better performance. Section III focuses on the low noise amplifier circuit design. Measurement results and comparisons to simulations are presented in section IV.

II. MM-WAVE COMPONENTS

The employed 90nm CMOS process has a f_t of 100 GHz which is largely layout independent. We have measured a

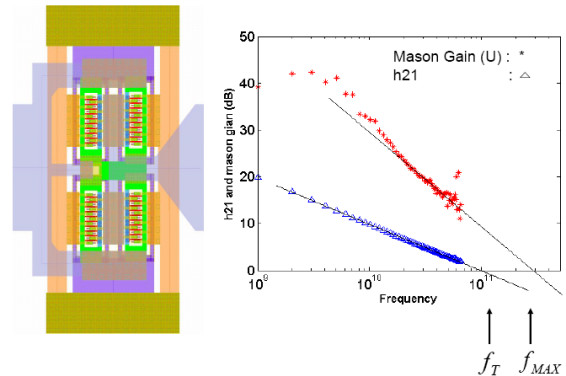


Fig. 1. Layout of a round table transistor with its performance metrics.

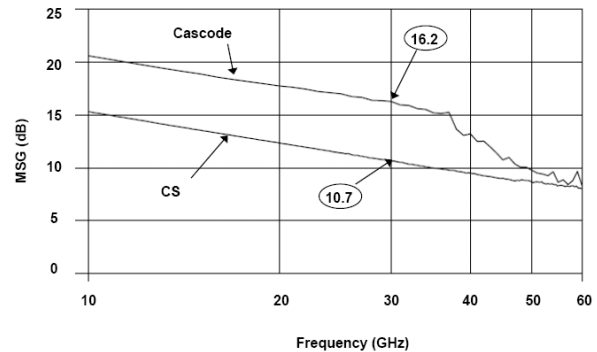


Fig. 2. Maximum stable gain for $40\mu\text{m}$ wide cascode and round-table common source transistors biased at $0.2\text{mA}/\mu\text{m}$.

carefully laid-out conventional transistor with 180 GHz of f_{max} . To improve the performance further, a custom layout was pursued. Since layout parasitics have a great impact on the f_{max} , the proposed layout minimizes key losses.

The “Round Table” structure, shown in Fig. 1, comprises of an arrangement of unit cells. Each unit cell is small with local substrate guard ring and contacts on both sides of the gate. The overall matrix of unit cells uses multipath connections to the gate, source and drain terminals. The parasitics can be decreased to a great extent such that an extrapolated $f_{max} = 300$ GHz is achieved [9]. Since minimization of gate and source resistance, the Round Table structure has also a better noise performance.

Fig. 2 shows maximum stable gain plots for $40\mu\text{m}$ wide

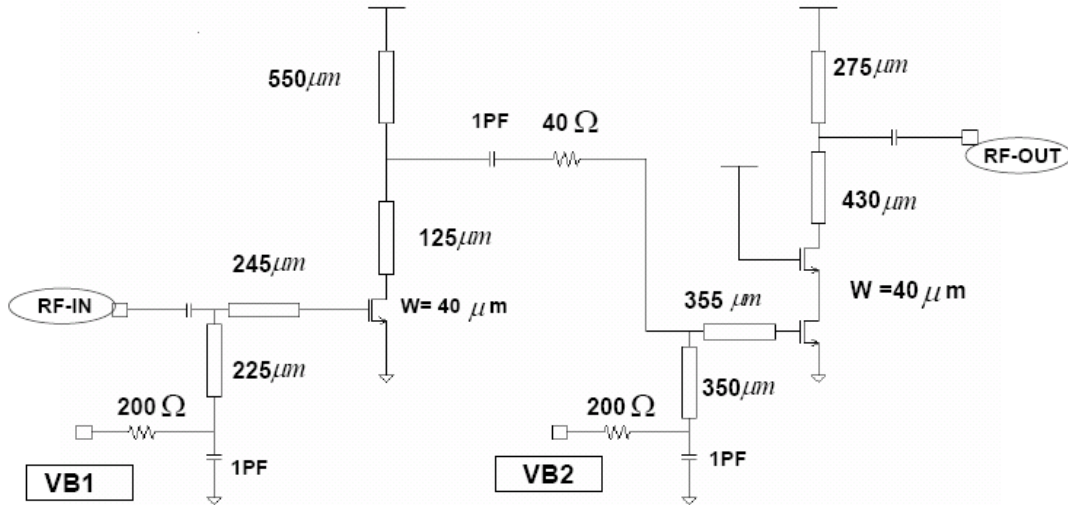


Fig. 3. Schematic of the LNA.

round table common source transistor and also a $40\mu\text{m}$ wide cascode device both biased at $0.2\text{mA}/\mu\text{m}$ which is a good compromise bias point for both high MSG and low NF_{min} . As depicted in the figure at 30GHz the CS has a $\text{MSG}=10.7\text{ dB}$ whereas the cascode has an MSG of 16.2dB .

For the matching networks we preferred transmission lines to loop inductors because the simulation of an inductor requires a detailed knowledge of the substrate as well as structures in close proximity to the inductor that contribute to return current paths. Additionally, due to the small dimensions of inductors at mm-wave frequencies, the size and effect of the interconnects will be crucial for their performance, which necessitates simulation of the entire layout. In contrast, the return current in a transmission line flows through a well defined path. The characteristic impedance of the line is thus highly predictable via EM simulations and there is close agreement between the measured and simulated data. In Fig. 4, S-parameter measurements confirms the correctness of this argument. For transmission lines, coplanar waveguide structure was used rather than microstrip lines due to the higher achievable Z_o . In order to lower the conductive loss, two top metal layers were strapped together to form the signal and ground lines. A $Z_o = 51\Omega$ was obtained by setting the signal line width to $10\mu\text{m}$ and gap spacing to $7\mu\text{m}$.

While MIM capacitors are optional in this process, they were avoided to keep costs low. Custom “finger” capacitors were designed for coupling and bypass. In these capacitors we took the advantage of the high density capacitance between different metal layers and between vias. A typical capacitor employed in the design has an area of $25\mu\text{m} \times 25\mu\text{m}$ and 914fF of capacitance, with a measured resonance frequency of 41 GHz .

III. CIRCUIT DESIGN

As depicted in the Fig. 2, up to 35 GHz the second pole does not have that much effect on the cascode gain. On the other hand, the cascode device has noticeably poorer noise performance which makes it unsuitable for the first stage of an amplifier. One approach to overcome this problem is to resonate out the junction capacitance [6], [10] but an alternative approach is to employ a single transistor amplifier as a first stage and remove the noise generated by the cascode device completely. Since gate resistance R_G has a great effect on the noise, we incorporate a round table structure in order to minimize this contribution as much as possible. A single transistor amplifier exploiting the round table structure and biased at $0.2\text{mA}/\mu\text{m}$ is used for the first stage. This round table device has simulated NF_{min} of 1.25dB at 30GHz .

Active devices are unconditionally stable at very low frequencies where capacitors are open and at very high frequency where the substrate and parasitic losses dominate. Due to the poor reverse isolation of a common source transistor at mm-wave frequencies, the first stage has stability issue and to resolve this problem a 40Ω stabilizing resistor is used between the two stages. The first stage has 12 dB of voltage gain and adding this resistor decreases the voltage level by 3dB so its effects on the overall noise performance is almost negligible and it increases the total NF by 0.5 dB .

To get enough gain and isolation, a cascode transistor was used for the second stage amplifier which is not as crucial for the overall noise figure. CPW structures were used extensively to realize the input, output and interstage matching networks as shown in the layout (Fig. 7). At mm-wave frequencies, the lengths are not prohibitively long and bending them saves even more area. Due to non-negligible gain at an unwanted

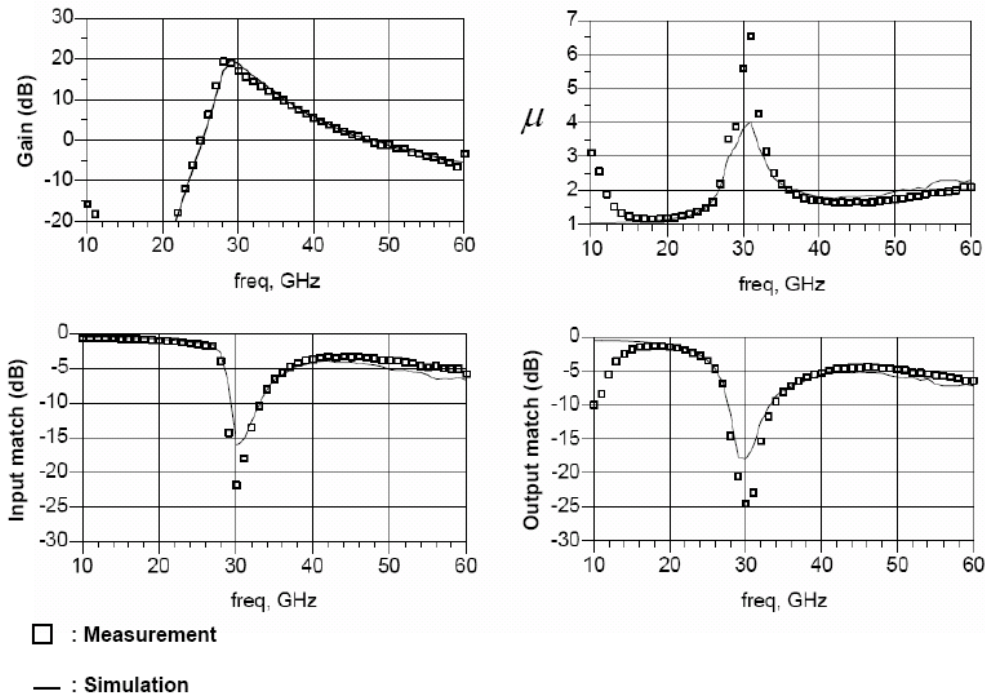


Fig. 4. Measured vs. simulated S-parameters and μ -stability factor.

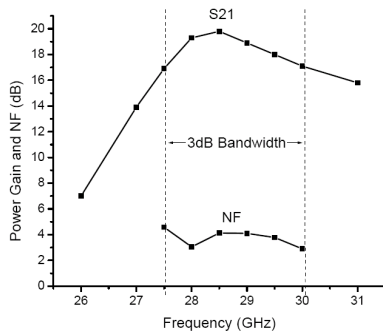


Fig. 5. Measured gain and noise figure.

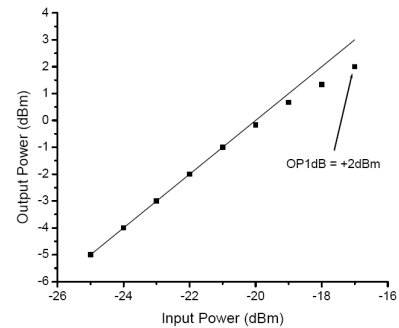


Fig. 6. Measured compression characteristics.

band around 5 GHz, 200 Ω resistors were used in the gate bias lines to de-Q the matching network and dampen the gain at 5 GHz completely. 1PF custom designed finger capacitors bypass these de-Q ing resistors at the desired frequency band.

IV. EXPERIMENTAL RESULTS

The fabricated prototype, shown in Fig. 7, has been characterized. Measurements were taken directly using wafer probes. The measured S-parameters are shown in Fig. 4, displaying good match between measurements and simulation. The amplifier has a peak gain of 20 dB at 28.5 GHz and 3-dB bandwidth from 27.6 GHz to 30.2 GHz. The amplifier is well matched, with input and output return loss better than 12 and 17 dB respectively over the 3dB bandwidth. The large signal and

distortion measurements verify +2 dBm of output power at the 1-dB compression point (input P1dB=-17dBm) and -7.5 dBm of IIP3.

Noise measurements were performed using the gain method. The input of the amplifier is matched and the output noise power is measured on a spectrum analyzer. The spectrum analyzer noise floor was too high (-140 dBm/Hz) for a direct measurement, so a second amplifier module with 28 dB of gain at 30 GHz was used to raise the output noise higher than the spectrum analyzer noise floor (around -127.5 dBm). The noise figure is calculated at a few points across the band and we found the minimum noise figure of 2.9 dB at 28 GHz (where the gain is close to its peak) and the NF is lower than 4.2 dB over the bandwidth of the amplifier (Fig. 5). The amplifier

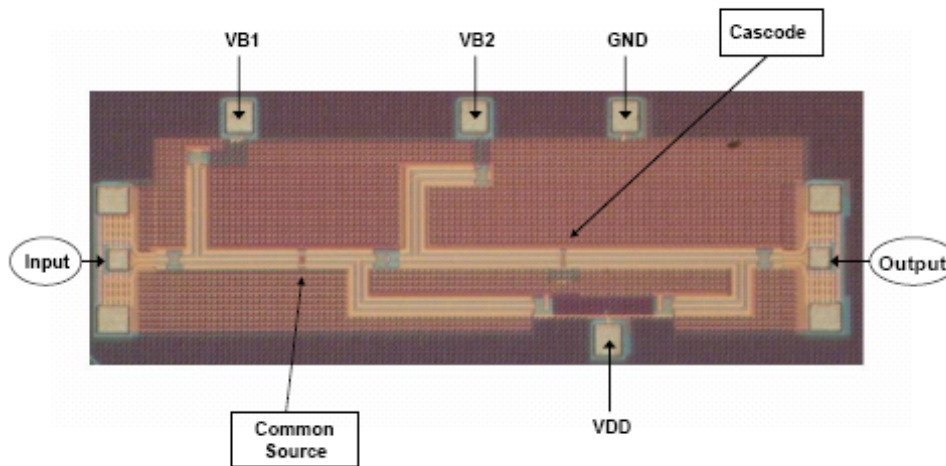


Fig. 7. Prototype die photo.

TABLE I
COMPARISON TO RECENTLY PUBLISHED MM-WAVE AMPLIFIERS.

| Ref. | This Work | [1] | [2] | [3] (amp1) | [6] | [7] |
|-----------------------|------------|------------|------------|------------|------------|-------------|
| Process | 90nm CMOS | 90nm SOI | 130nm CMOS | 90nm CMOS | 90nm CMOS | 130nm CMOS |
| Peak Gain (dB) | 20@28.5GHz | 11.9@35GHz | 20@43GHz | 5.8@20GHz | 18.6@33GHz | 8.4@26.2GHz |
| Input Match (dB) | -12 | -6 | -14 | -10 | -8 | -10 |
| Output Match (dB) | -17 | -18 | -17 | -18 | -8 | -10 |
| NF (dB) | 2.9@28GHz | 3.6@35GHz | 6.3@41GHz | 6.4@20GHz | 3@33GHz | 4.8@26.2GHz |
| OP1dB (dBm) | 2 | 4 | 4 | 1 | N/A | N/A |
| IIP3 (dBm) | -7.5 | N/A | -5.5 | -2.8 | N/A | -13 |
| Power Dissipation(mW) | 16.25 | 40.8 | 36 | 10 | 10 | 0.8 |
| Area (mm^2) | 0.67 | 0.18 | 0.525 | 0.56 | .856 | N/A |

consumes 16.25 mW of power from a 1 V supply voltage. The current is nearly evenly divided between the stages.

Table I summarizes the performance of recently reported mm-wave amplifiers. The amplifier presented in this work has good gain, matching and noise performance while dissipating only 16.25mW of power. The linearity is satisfactory for most wireless applications, which is achieved with a low supply voltage of 1 V (Fig. 6).

V. CONCLUSION

A 30 GHz low noise amplifier was implemented in a standard digital 90nm CMOS process. Good performance was achieved through careful device and layout optimizations without utilizing RF/analog process options. A round table transistor structure was used to realize higher f_{max} and lower NF_{min} . Low loss CPW lines with two top metal layers strapped together and custom finger capacitors were used for the matching and bypassing networks. Measurement results confirm simulations and the design methodology. The LNA achieves 20 dB of peak gain at 28.5 GHz and a minimum NF of 2.9 dB while consuming 16.25 mW from a 1 V supply.

VI. ACKNOWLEDGEMENT

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