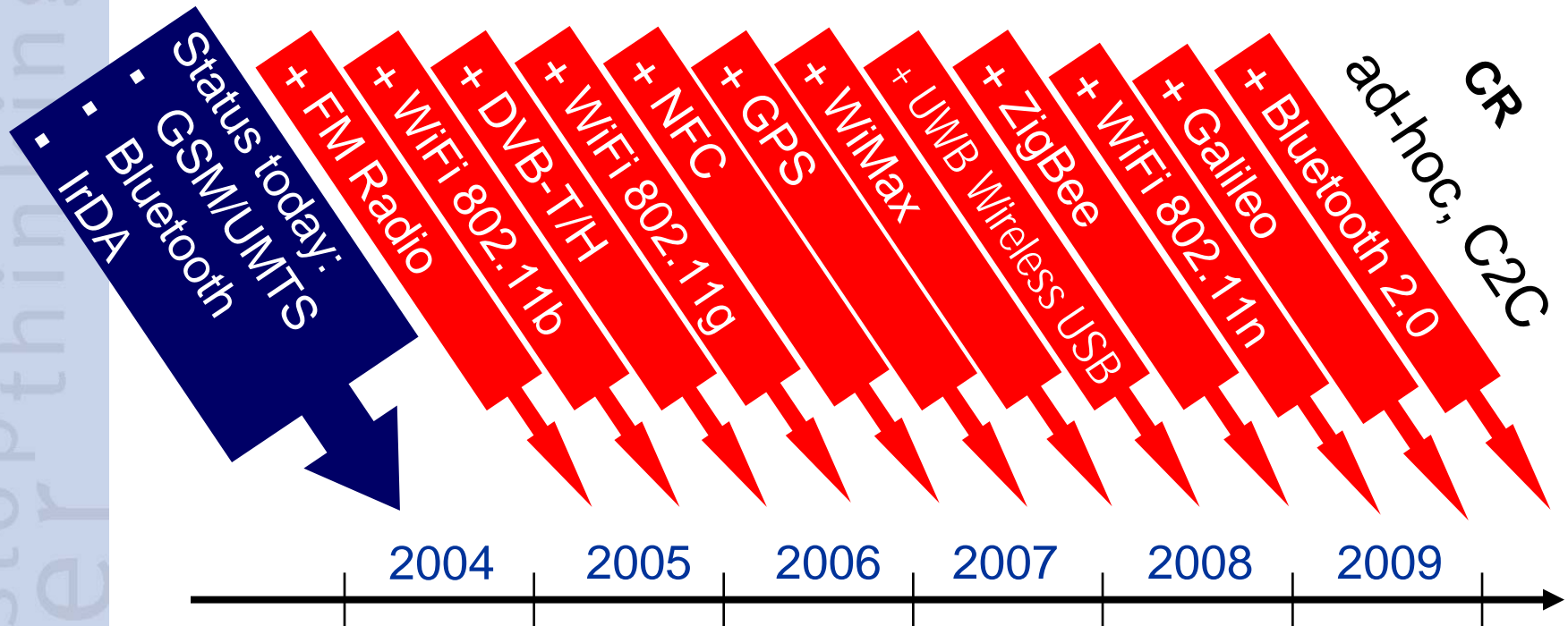

Common Framework for Application and Architecture Modeling

- DSE for multi-standard radios
- proposal

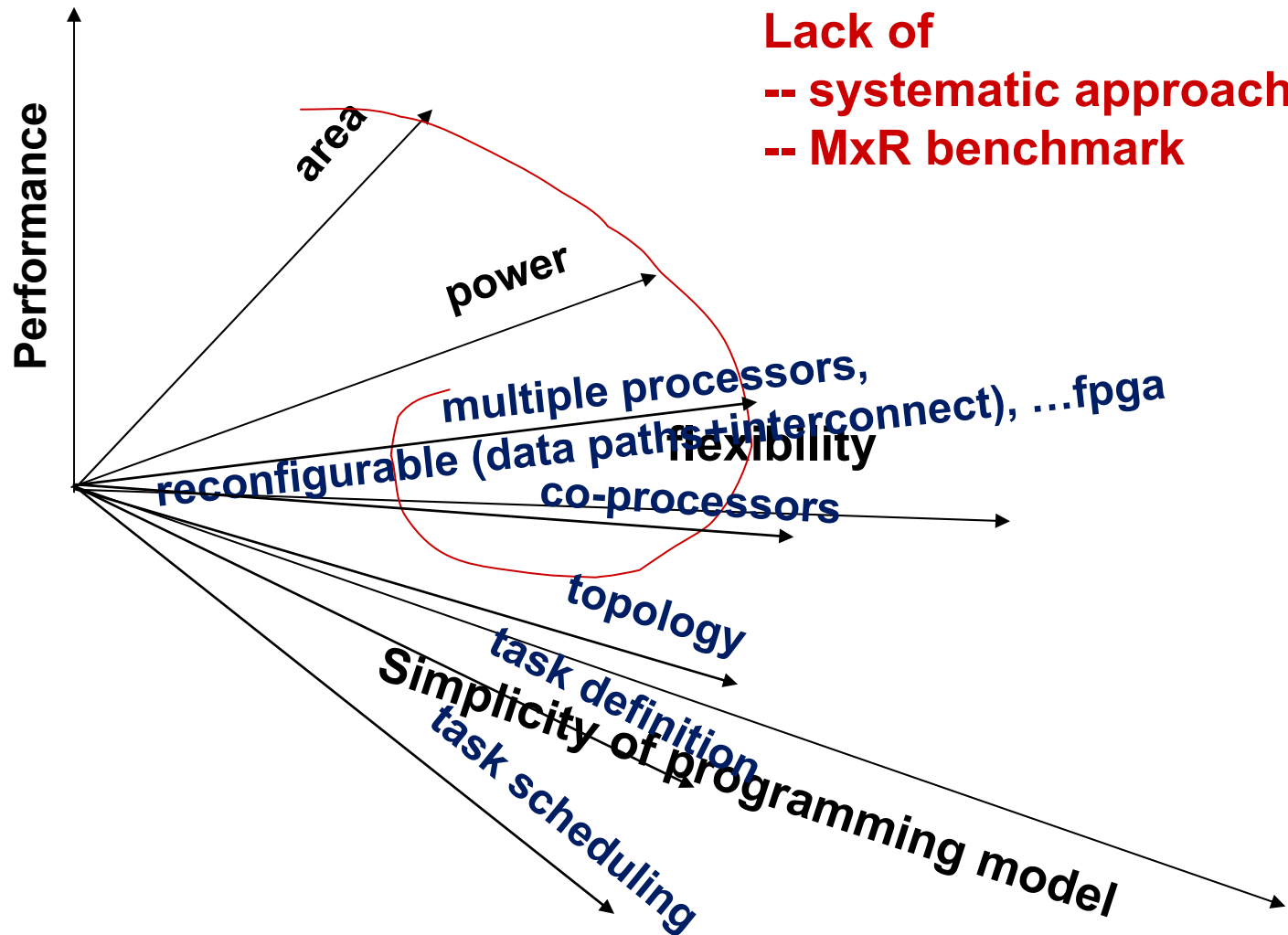
CR is part of multi-standard radio



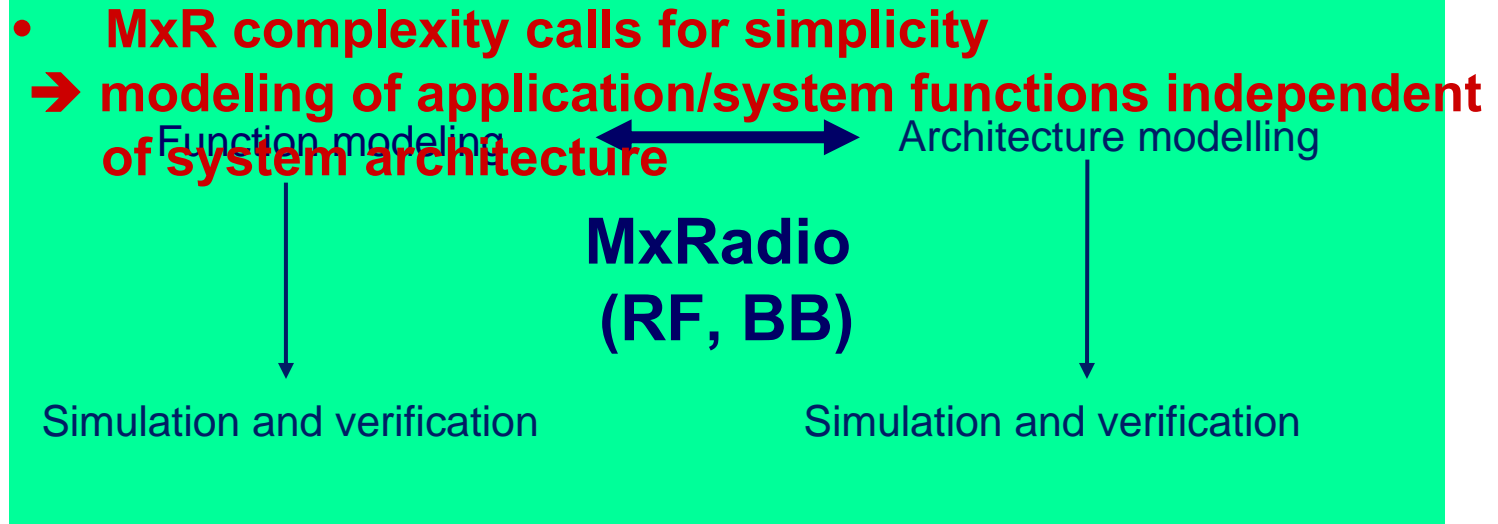
- ▶ WiFi
 - ▶ IEEE 802.11b: 11Mb/s wireless LAN @ 2.4GHz (< 100m)
 - ▶ IEEE 802.11g: 54Mb/s wireless LAN @ 2.4GHz (< 100m)
 - ▶ IEEE 802.11a: 54Mb/s wireless LAN @ 5GHz (< 100m)
- ▶ UWB (IEEE 802.15.3a): 480Mb/s wireless USB2.0 (~ 1m)
- ▶ WiMax (IEEE 802.16d/e): ~10Mb/s broadband wireless access
- ▶ NFC: Near Field Communications (RF-ID,...)
- ▶ ZigBee: (IEEE 802.15.4) Sensor Networks, remote control
 - ▶ Bluetooth Version 1: 723 kb/s
 - ▶ EDR: 2.2 Mb/s

stop thinking
Never

Architect's Challenge



Towards a Systematic Approach



Application/System Function Modeling:

- Describing functional components and their interactions in a signal processing chain, control data and timing driven process
 - **modeling of application/system functions independent of system architecture**
 - Verification of functions for well-defined scenarios
 - reference, implementation independent
 - **→ Re-use over technology platforms and product classes**
 - Standardization of interfaces between the parties/OEM/ODM
- Statistics of functions and communications**

Never stop thinking

Information from Application/System Function Modeling (1)

List of

- basic functional components
- communication lines

List of frequency of occurrence of

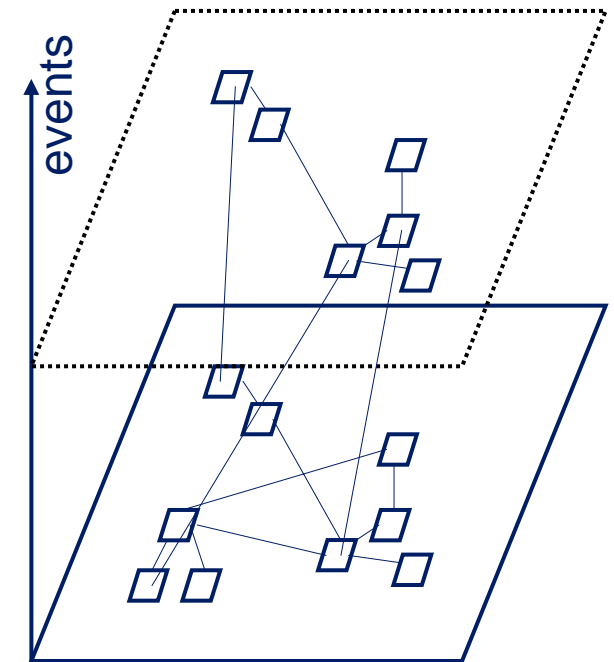
- basic functional components
- communicating tuples, tripels

List of

- clusters of communicating bas. func. comp.
- clusters of clusters ...

List of sequence of

- bas. func. comp., tuples
- clusters, ...



Information from Application/System Function Modeling (2)

bas. func. comp. → application-specific instruction,
selected configuration of reconfigurable data path
cluster of FPGA cells

cluster of
bas. func. comp. → multiple instructions, VLIW instruction
sel. conf. of multiple rec. data paths
cluster of cluster of FPGA cells

cluster of clusters → thread

sequence of

-- bas. func. comp.	→ task,	}	executed on
-- cluster of bfc.	process,		
-- cluster of clusters	program		
			-- processors
			-- rec. dat paths,
			-- FPGAs

Design Criteria

area

power

scalability

**flexibility = reusability in future designs,
fixing errors**

simplicity of programming model

- **weights**
 - **priorities**
- } → **architecture**

Case 1: $\text{area} < \text{bound}$ search for lowest power architecture

- Start from entry point



- multiplex bas. func. comp. in space and time

→ **area reduced,
power consumption increased**

- if $\text{area} > \text{bound}$, introduce new func. comp.
more fine-grain than bas. func. comp.

→ **area reduced,
power consumption increased,
some flexibility**

Case 2: area, power consumption < bounds search for most flexible architecture

- Start from entry point



**high flexibility,
area too high,
power consumption too high**

- replace several clusters of fpga cells
by rec. data path and interconnect



**flexibility reduced,
area reduced,
power consumption reduced**

- if area > bound, replace by new rec. dp+ic
more coarse grain than previous ones



**flexibility further reduced,
area further reduced,
power consumption further reduced**

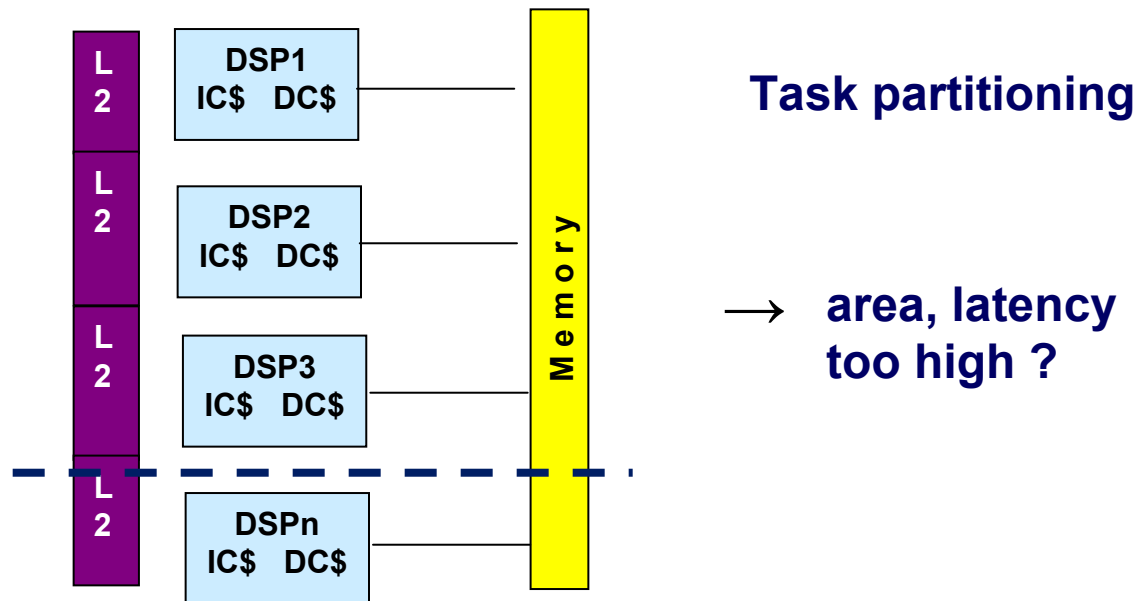
Case 2b: area, power consumption < bounds search for most flexible architecture

- Start from entry point

1 GHz DSP
IC\$ DC\$
I/O Bwdth

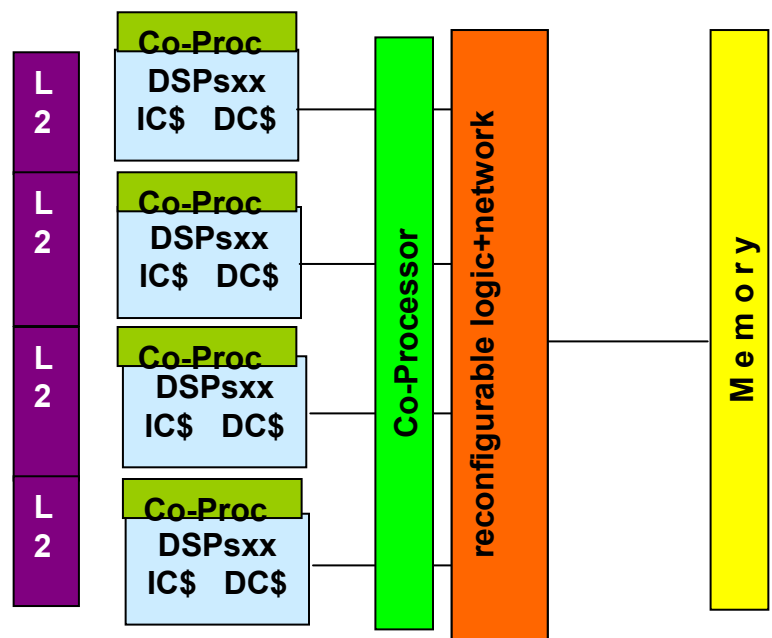
→ MHz, Cache, L2, Mem, I/O

- choose smallest array of GP processing units with highest clock that fits power budget



Design Space Exploration

- deviate minimally from GP ISA

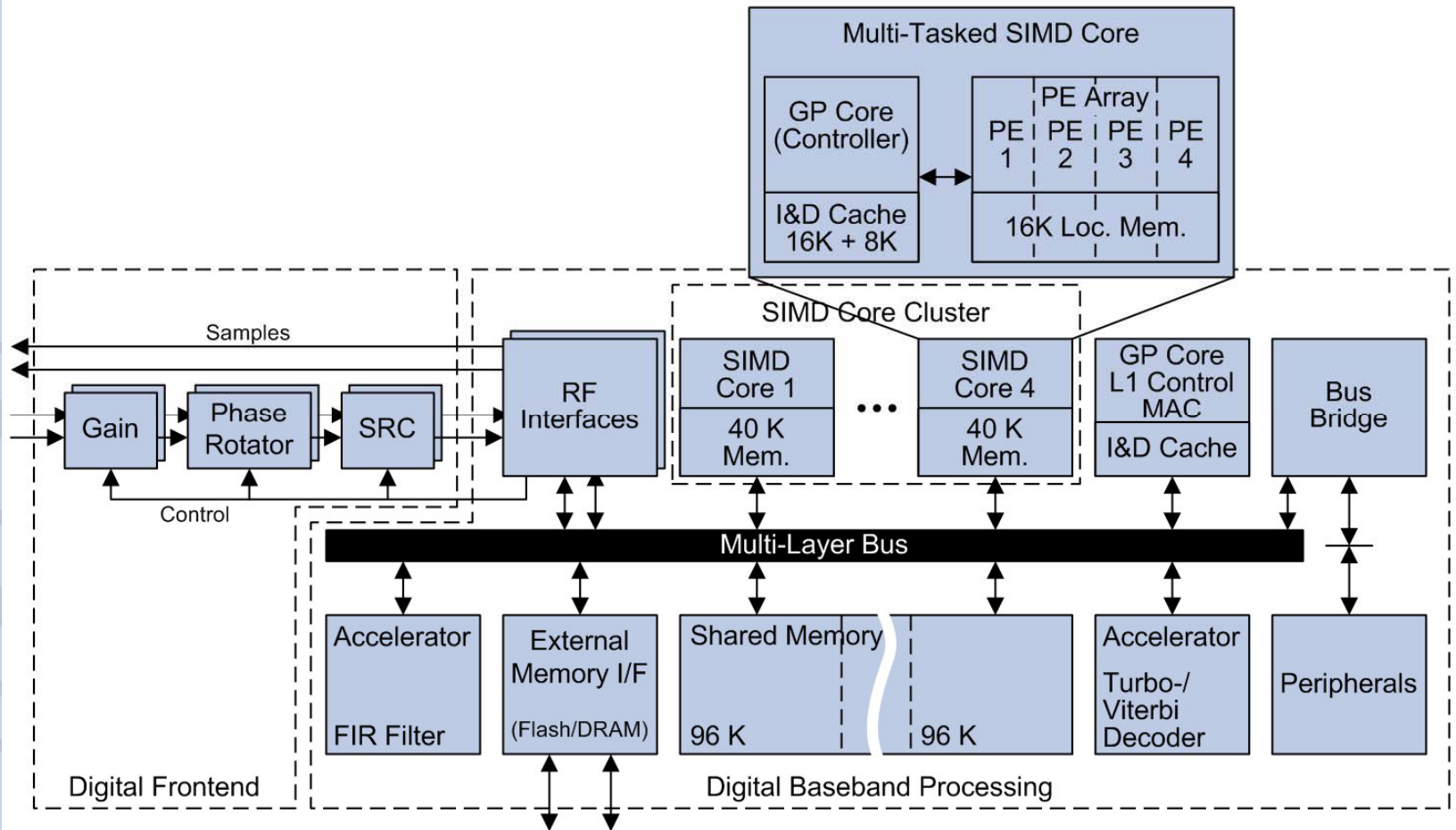


result depends on initial task-partitioning

→ cost function for throughput and communication

BB Platform

Features:
 UMTS, EDGE, GSM, GPRS, 802.11a/b/g (2 concurrently)
 L90, 2150 kG, 704 KB



Application-driven Architecture Development

Product class

Design criteria

Entry point to DSE

step-by-step

DSE, concurrency

→ mapping problem

Virtual prototype

Customer Interface

Code generation

Application description

Application verification

for example: **METROPOLIS**

separate modeling of function & architecture
(computation and communication,
function and constraints,
synchronization mechanisms) ✓

iterative refinement of modeling ✓

code generation for architecture platforms (✓)

interface to formal verification (✓)

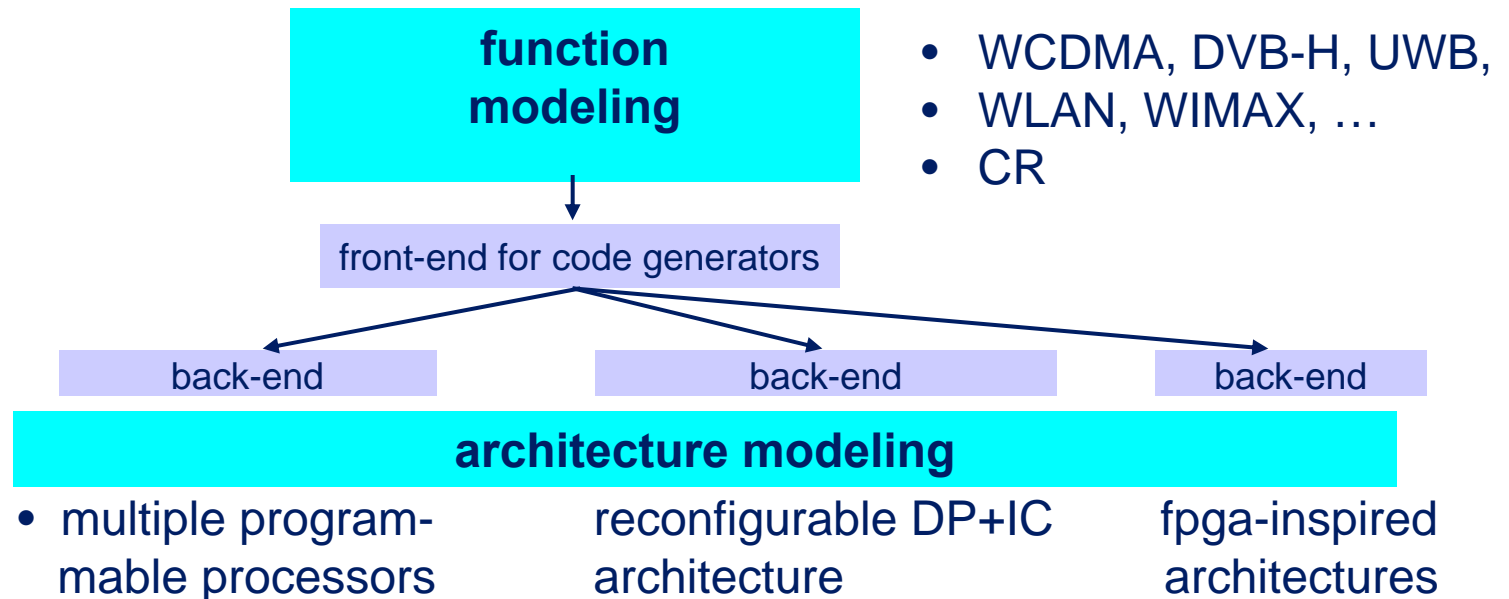
interface to statistics of func. comm.

**description
of essential MxR functions
and real-time behaviour**

**→ benchmarks,
programming language**

stop thinking
Never

Proposal



Common Research Agenda:

- benchmarks
- real-time in f&a space
- common rules for modeling
- systematic design space exploration
- code generators
- „Future-proof“ framework for Function&Architecture Modeling (Matlab, Simulink, Metropolis ...?)

Metropolis – Function Modeling

- **offered today:**
 - **meta modeling language for functional decomposition (Java based)**
 - **interconnection of components by coupled events**
 - **interface to other tools (via abstract syntax tree or .mmm file)**
 - **elaboration tool for analyzing hierarchies**
 - **syntax for constraints (timing, power and interaction constraints), to be handled by quantity manager**
 - **support of formal verification via Spin (e.g. for finding certain types of deadlocks)**
- **needed in the future:**
 - **profiling support, recognition of temporal patterns**
 - **import of Simulink description, interaction with other tools**
 - **functional lib**
 - **graphical support**

Metropolis – Architecture Modeling

- **offered today:**
 - **component lib (processor, memory, DMA)**
 - **schedule generation based on constraints**
 - **generation of SystemC simulation code**

- **needed in the future:**
 - **support of code generation for parallel systems (interfaces to tools)**
 - **graphical support**
 - **profiling support, recognition of temporal patterns**