

9.5 Power Manager

The SA-1100 contains power management logic that controls the transition between three different modes of operation: run, idle, and sleep. These modes are used to reduce processor power consumption at times when some functions are not needed, or when the system's power supply is low or out of regulation. Each of the respective modes is associated with a reduced level of power consumption. Idle mode is entered via software. Sleep mode is entered either via software or by asserting one of two input pins that indicate a power supply fault. Idle mode is exited through an interrupt. Sleep mode is exited through a preprogrammed wake-up condition. Both modes may be exited in extreme cases via hardware reset. If none of the power management modes is active and the SA-1100 is out of reset, then it is said to be in run mode.

9.5.1 Run Mode

Run mode is the normal operating mode of the SA-1100: all power supplies are enabled, all clocks are running, and every on-chip resource is functional. This is the normal state of operation for the processor while it is executing code. Under usual conditions, the processor enters run mode after successful power-up and reset of the part.

9.5.2 Idle Mode

Idle mode allows a software application to stop the CPU when not in use, while continuing to monitor interrupt service requests both on or off-chip. When an interrupt occurs, the CPU is reactivated. During idle mode, the SCM, PM, and MPCM are each fully operational.

In idle mode, the CPU clock is stopped. Since the SA-1100 is static, all CPU state information is saved. This allows the part to be switched back to run mode, starting operation exactly where it left off. During idle mode, all other on-chip resources are active, including: all system unit modules (real-time clock, operating system timer, interrupt controller, general-purpose I/O, and power manager); all peripheral unit modules (DMA controller, LCD controller, serial controller 0-4); and all memory controller resources. The PLL also remains in lock so that the part can be brought out of idle mode quickly when an interrupt occurs.

9.5.2.1 Entering Idle Mode

Idle mode is entered while in run mode by executing a three instruction sequence consisting of the privileged on-chip coprocessor 15 instruction 'disable clock switching', a load from a noncacheable memory location (C=B=0), and the privileged on-chip coprocessor 15 instruction 'wait for interrupt'. This sequence must reside in the first three words of an instruction cache line, which requires that the linker align the idle mode instruction sequence on an eight word boundary. Idle mode is entered by following the exact code sequence:

```
AREA | Idle$$Code |, CODE, READONLY, ALIGN=5
                                ;Aligned to 8 word boundary
                                ;p15 = coprocessor 15
                                ;r0 = register 0 (contents not used)
                                ;c15 = test, clk, and idle cntl register
                                ;c2 = CRm = 0b0010
mcr p15, 0, r0, c15, c2, 2      ;2 = OPC_2 = 0b010
ldr r0, <r1>                    ;<r1> points to non-cachable mem loc
mcr p15, 0, r0, c15, c8, 2      ;c8 = CRm = 0b1000
```

9.5.2.2 Exiting Idle Mode

Any enabled interrupt from the system unit or peripheral unit will cause a transition from idle mode back to run mode. Note that the interrupt controller (ICMR) mask register is ignored during idle mode, meaning that an interrupt does not need to be unmasked to bring the SA-1100 out of idle. When an interrupt occurs, the CPU clocks are reactivated, the wait for interrupt instruction is completed, and run program flow resumes.

A transition from idle to run mode can also occur by asserting the nRESET pin or if OSMR<3> is configured as a watchdog and a match occurs that causes the assertion of reset. Since the watchdog timer (if enabled) is functional during idle, care must be taken to set the watchdog match register far enough in advance to ensure that another interrupt is guaranteed to bring the SA-1100 out of idle before the watchdog reset occurs. It is recommended that either an RTC alarm or another OS timer channel be used for this purpose.

When in idle mode, if the BATT_FAULT and/or VDD_FAULT pins are asserted, the SA-1100 enters sleep mode.

9.5.3 Sleep Mode

Sleep mode offers the greatest power savings to the user and consequently the lowest level of available functionality. In the transition from run or idle to sleep mode, the SA-1100 performs an orderly shutdown of on-chip activity, applies an internal reset to the processor, and then negates the PWR_EN pin indicating to the external system that the VDDI (1.5-V supply) should be driven to zero volts. Internally, this switches off the power to the majority of the processor at this time. (The VDDX I/O voltage supply must remain powered during sleep.) Running off the 32.768-kHz crystal oscillator, the sleep state machine watches for a preprogrammed wake-up event to occur, after which it asserts PWR_EN (to reestablish the VDDI power supply), and steps through an orderly wake-up sequence. When the power supply and clocks are stable, the power manager brings the SA-1100 out of reset. Status bits in the power manager GPIO sleep state register (PGSR) may be read to indicate to software that the reset was due to sleep mode.

9.5.3.1 CPU Preparation for Sleep Mode

In preparation for sleep mode, software should initialize the power manager GPIO sleep state register (PGSR) and the power manager wake-up enable register (PWER). Also, the GPIO falling-edge detect and GPIO rising-edge detect enable registers (GFER and GRER) should be written with the appropriate values. The OPDE bit in the power manager configuration register (PCFR) should also be programmed with the desired value.

9.5.3.2 Events Causing Entry into Sleep Mode

Sleep mode can be entered in one of two ways: via software or a power supply fault. Entry into sleep mode via software is accomplished by setting the force sleep bit in the power manager control register (PMCR). This bit is set by software and cleared by hardware during sleep. When the SA-1100 wakes up from sleep, this bit is already cleared.

Entry into sleep via a power supply fault is caused by the assertion of either the VDD_FAULT or BATT_FAULT pins. The VDD_FAULT pin should be used to indicate that the main power supply is out of regulation. The BATT_FAULT pin should be used to indicate that the battery has been removed or is low. These pins have identical operation for the purpose of entering sleep mode. They have different implications during the wake-up sequence as described in the following section.

9.5.3.3 The Sleep Shutdown Sequence

The sleep state machine begins the shutdown sequence. This sequence consists of three steps.

- In the first step, the following actions occur:
 - a. Power manager switches the GPIO output pins to their sleep state. This sleep state is programmed in advance by loading the power manager GPIO sleep state register (PGSR) into the GPIO output data register. (See the Section 9.1, “General-Purpose I/O” on page 9-1.)
 - b. The DRAMs are placed into self-refresh mode. The memory controller finishes whatever memory operation might be in progress and then drives the RAS<3:0> and CAS<3:0> pins low.
 - c. If the sleep sequence was entered due to the assertion of VDD_FAULT or BATT_FAULT, the possible wake-up sources are reset from what was programmed by software to their "fault state". The fault state is to allow a transition only on GP<0> and GP<1> to act as a wake-up event.
- In the second step of sleep shutdown, the following actions occur:
 - a. All potential wake-up sources are cleared. This involves clearing all the GPIO edge detect status bits and clearing the RTC alarm interrupt bit. These bits are cleared to prevent latent status bits from causing an immediate wake-up. This functionality is provided to cover the situation of entering sleep due to a power fault because the CPU does not have the ability to prepare for the entry into sleep.
 - b. An internal reset is applied to the SA-1100. All units are reset and the RESET_OUT pin is asserted.
- In the third step of sleep shutdown, the following actions occur:
 - a. The 3.686-MHz oscillator is stopped. This action is dependent on the state of the oscillator power-down enable bit (OPDE) in the power manager configuration register (PCFR). If this bit is set, then the oscillator is stopped during sleep, resulting in greater power savings. If the bit is cleared (the power-on reset state), then the oscillator continues to run during sleep and results in a faster wake-up sequence.
 - b. The PWR_EN pin is negated. The external system must respond to this negation by disabling the VDDI power supply. In contrast to the SA-110, the SA-1100 systems are not required to drive VDDI to zero volts in sleep. However, the power supply should be disabled to prevent power consumption.

Each step in the sleep shutdown sequence takes one cycle of the 32.768-kHz clock (~30 microseconds).

9.5.3.4 During Sleep Mode

During sleep mode, the SA-1100 watches for preprogrammed wake-up events. These events are either programmed by the CPU prior to setting the force sleep bit or by the power manager when a fault condition is detected.

9.5.3.5 The Sleep Wake-Up Sequence

When a valid wake-up event is detected and there is no BATT_FAULT, the SA-1100 begins a wake-up sequence. If BATT_FAULT is asserted, then the wake-up event is ignored. VDD_FAULT is always ignored at this time because the VDDI supply is disabled at this time. The wake-up sequence occurs in three steps.

- In the first step of the wake-up sequence, the following actions occur:
 - a. The PWR_EN pin is asserted, indicating that the external supply must apply power on the VDDI pins.
 - b. An internal timer begins to time the power ramp. This timer waits for approximately 10 ms.
 - c. The 3.686-MHz oscillator is enabled for operation if it was originally programmed to be disabled.
 - d. If BATT_FAULT is asserted at any time during the sleep wake-up sequence, the power manager transitions back to sleep mode through the fault state.
- In the second step of the wake-up sequence (after the power ramp timer has expired), the following actions occur:
 - a. A second internal timer begins to time the 3.686-MHz oscillator as it begins to ramp up to speed. This timer waits for 150 ms. If the OPDE bit in the PCFR is zero, then the oscillator was never disabled and this timer is not used. In this case, the power manager transitions to the third step directly without waiting for the oscillator timer to complete.
 - b. If BATT_FAULT or VDD_FAULT is asserted at any time during the oscillator ramp, the power manager transitions back to sleep mode through the fault state.
- In the third step of the wake-up sequence (after the 3.6864-MHz oscillator is stabilized), the following actions occur:
 - a. The SA-1100 internal reset is negated and the CPU begins a normal boot sequence.
 - b. The RESET_OUT pin is negated, indicating that the SA-1100 is about to perform a fetch from the reset vector location.

During the fault state entered through the assertion of VDD_FAULT or BATT_FAULT, the following actions occur:

- All potential wake-up sources are cleared (all GPIO edge detects and the RTC alarm interrupt).
- The power manager wake-up source register (PWER) is loaded with 0x0000 0003 and bits 0 and 1 of the GFER and the GRER (see the Section 9.1, “General-Purpose I/O” on page 9-1) are set. This limits the potential wake-up sources to a rising or falling edge on GP<0> or GP<1>. This wake-up fault state is provided to prevent spurious events from causing an unwanted wake-up during a low battery or shorted power supply situation. This fault state setting of PWER, GRER, and GFER registers is also the default state of the registers after a hardware reset.

9.5.3.6 Booting After Sleep Mode

When the SA-1100 boots after sleep mode (or at any other time), it must examine the reset controller status register (RCSR) to determine why it just booted. This register has bits to indicate sleep reset, software reset, watchdog reset, or hardware reset (assertion of nRESET). See the Section 9.6, “Reset Controller” on page 9-41 for more details on reset.

Next, software should examine the power manager sleep status register (PSSR) to determine why it was in sleep. This register has bits to indicate whether a VDD_FAULT, BATT_FAULT, or force sleep bit has been asserted since the register was last cleared. It is possible for multiple bits to be set in this register.

Also, the SA-1100 provides the power manager scratchpad register (PSPR) for saving any general processor state during sleep. This register may be written by the processor and the contents will survive sleep mode. The bits in this register are not explicitly used by the SA-1100, but may be used by software to index into ROM space to retrieve memory controller configuration, for example.

Note: The nRESET pin must not be asserted during sleep mode if the DRAM contents are to be preserved. The assertion and subsequent negation of nRESET during sleep mode causes the SA-1100 to clear the FS bit in the force sleep register, assert PWR_EN, time the PLL lock sequence, and subsequently negate the internal reset signal. This causes the SA-1100 to perform a normal boot sequence because all information about the previous sleep state is lost.

9.5.3.7 Reviving the DRAMs from Self-Refresh Mode

Because the DRAMs are placed in self refresh prior to the sleep mode shutdown, their contents are preserved during sleep. After exiting sleep, software must reconfigure the DRAM control registers, which lost power during sleep mode, and then take the DRAMs out of self-refresh mode. Clearing the DRAM hold (DH) bit in the power management status register (PMSR) will cause the RAS<3:0> and CAS<3:0> pins to return to the negated state (high) in preparation for a DRAM access.

9.5.4 Notes on Power Supply Sequencing

On the SA-1100, as on the SA-110, it is important that VDDX (3.3 V nominal) power-up occur before VDDI (1.5 V nominal). One approach to ensuring this sequencing is to power the 1.5-V supply using the 3.3-V supply. On the SA-1100, a second simple option is available. If the PWR_EN output is used to enable the 1.5-V supply, the SA-1100 will enforce the required sequencing by holding PWR_EN deasserted until the 3.3-V supply is sufficiently high.

9.5.5 Assumed Behavior of an SA-1100 System in Sleep Mode

The assumed model of an SA-1100 system in sleep mode is one in which the system is relatively quiet. In particular, there should be no gratuitous switching on of the SA-1100 input pins. Although there will be some switching in GPIOs to bring the processor out of sleep and potentially on the VDD_FAULT and BATT_FAULT pins, the switching is a low-frequency activity and usually brings the SA-1100 out of sleep mode.

The major concern is for power dissipation in sleep and requirements for the power supplies on the processor during sleep. The SA-1100 generates these supplies using several on-chip regulators with limited current capacity. Excessive activity on-chip pins might load these regulators beyond their capacity and result in droop of the on-chip supplies. One example is that of a component tied to one of the GPIO pins that constantly transmits to the processor. If the system design indicated that activity from this detector should not bring the SA-1100 out of sleep, the transitions from this GPIO might result in switching in the processor that would exceed the sleep current limit. This concern exists regardless of whether the GPIO is enabled as a wake-up source.

Figure 9-3 shows the three power-related modes of the SA-1100 and the actions that cause transitions between the modes. Table 9-2 summarizes what power and clock supplies are used by each module within the SA-1100, as well as the status of the power and clock supplies to each unit during each of the three power-related modes.

Figure 9-3. Transitions Between Modes of Operation

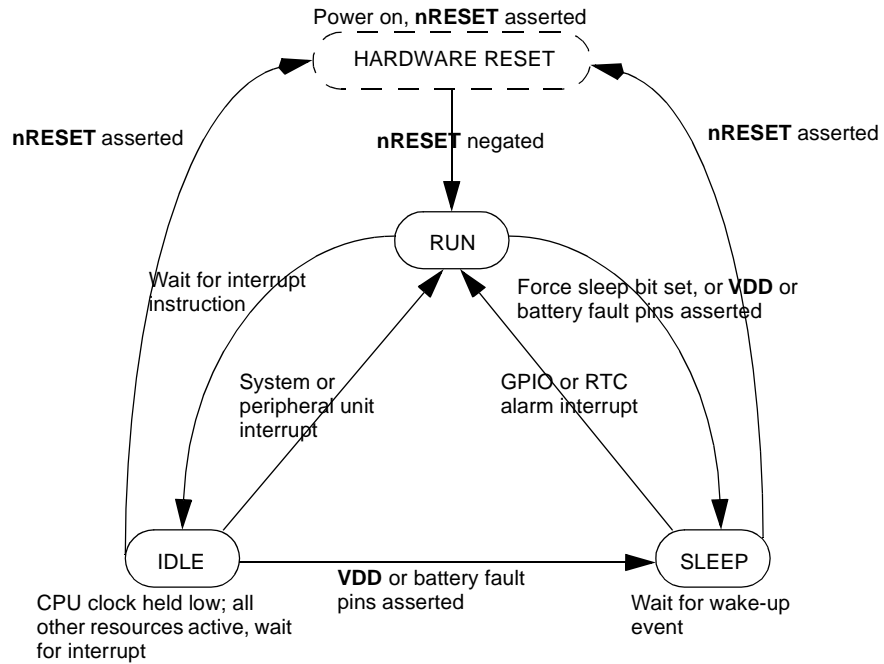


Table 9-2. SA-1100 Power and Clock Supply Sources and States During Power-Down Modes

Module	Power Management Mode							
	Supply Source		Run		Idle		Sleep	
	Pwr	Clk	Pwr	Clk	Pwr	Clk	Pwr	Clk
CPU	VDD	3.6864 MHz	On	Running	On	Running	Disabled	Stopped
MMUs (I&D)								
Write buffer								
Read buffer								
JTAG								
OS timer								
LCD controller								
Serial channel 0-4								
Memory and PCMCIA control	VDDX	32.768 kHz	On	Running	On	Running	On	Running
Real-time clock								
Interrupt controller								
Power manager								
General-purpose I/O								
Pin pads								

9.5.6 Pin Operation in Sleep Mode

The SA-1100 pins are categorized by the following types based on their behavior during sleep mode:

Type 1 – These pins are outputs and are driven low during sleep. These pins hold their state after sleep mode is exited until the DRAM_control_hold bit in the PSSR is cleared.

Type 2 – These pins are outputs and are normally driven to a one in sleep. To support systems that power down external devices, these pins can also be tristated in sleep through the use of the FLOAT_STATIC and FLOAT_PCMCIA bits in the PCFR. See the Section 9.5, “Power Manager” on page 9-26.

Type 3 – These pins are I/Os. When programmed as outputs, they can be actively held high or low during sleep. When programmed as inputs, they are actively sampled by the SA-1100.

Type 4 – These pins are I/Os but become inputs during sleep. They can be programmed to hold the pin state at a zero or can be tristated. The receivers on these pins are disabled during sleep. These pins hold their state after sleep mode is exited until either the peripheral_control_hold bits in the PSSR are cleared.

Type 5 – These pins are outputs and are actively driven during sleep.

Type 6 – These pins are outputs and are tristated during sleep.

Type 7 – These pins are inputs and are actively sampled during sleep.

Type 8 – These pins are inputs and are not observed during sleep; the receiver is disabled.

Type 9 – These pins are analog inputs and outputs, and are always active.

Table 9-3. Pin State During Step

Pin Name	Type	Pin Name	Type	Pin Name	Type	Pin Name	Type
A<25:0>	1	nPREG	1	RXD_2	4	nRESET_OUT	1
D<31:0>	1	L_DD<7:0>	4	TXD_3	4	nTRST	8
nCS<3:0>	2	L_FCLK	4	RXD_3	4	TDI	8
nOE	2	L_BIAS	4	GP<27:0>	3	TDO	6
nWE	2	TXD_C	4	ROM_SEL	8	TMS	8
nRAS<3:0>	1	RXD_C	4	PXTAL	9	TCK	8
nCAS<3:0>	1	SCLK_C	4	PEXTAL	9	TCK_BYP	7
nPIOW	2	SFRM_C	4	TXTAL	9	TESTCLK	7
nPIOR	2	UDC+	4	TEXTAL	9	VDD	—
nPCE<2:1>	2	UDC-	4	PWR_EN	5	VDDX	—
nIOIS16	2	TXD_1	4	BATT_FAULT	7	VSS	—
nPWAIT	2	RXD_1	4	VDD_FAULT	7	VSSX	—
PSKTSEL	1	TXD_2	4	nRESET	7	—	—

9.5.7 Power Manager Registers

The power manager is controlled through eight 32-bit registers. The power manager control register (PMCR) is used to allow software invocation of sleep mode. The sleep status register (PSSR) contains status bits that indicate why sleep mode was invoked. The power manager scratchpad register (PSPR) is a general-purpose register used to store processor data during sleep. The power manager wake-up enable register (PWER) is used to program the desired wake-up sources in the system. The power manager general configuration register (PCFR) contains bits used to control various configurable functions within the SA-1100. The power manager PLL configuration register (PPCR) allows the user to change the PLL operating frequency. The power manager GPIO sleep state register (PGSR) is used to program the value loaded onto GPIO outputs when the SA-1100 transitions into sleep mode. The power manager oscillator status register (POSR) contains a single bit that indicates whether the 32.768-kHz oscillator has stabilized after a hardware reset.

9.5.7.1 Power Manager Control Register (PMCR)

Sleep mode is invoked by setting the force bit within the power manager control register (PMCR). The force bit is automatically cleared upon exiting sleep mode or when a hardware reset occurs. Writing zero to the force bit has no effect. For reserved bits, writes are ignored and reads return zero. This register should be protected by programming MMU permissions. The following table shows the PMCR.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
R/W	Reserved																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R/W	Reserved															SF	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
0	SF	Sleep force. 0 - Do not force invocation of sleep mode. 1 - Force invocation of sleep mode. Note: This bit is cleared on wake-up or a hardware reset.
31..1	—	Reserved.

9.5.7.2 Power Manager General Configuration Register (PCFR)

The PCFR contains bits used to configure various functions within the SA-1100. The OPDE bit, if set, allows the 3.6864-MHz oscillator to be disabled during sleep mode. This bit is cleared on the assertion of nRESET. The FP and FS bits control the state of the PCMCIA control pins and the static memory control pins during sleep. The following table shows the bit-field definitions for this register. The FO bit forces the SA-1100 to assume that the 32-kHz oscillator is stable instead of waiting for the requisite 2–10 seconds using an internal counter. This function is primarily useful for "warm" hardware resets where the oscillator is already stable when the processor comes out of reset.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	Reserved												FO	FS	FP	OPDE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
0	OPDE	3.6864-MHz oscillator power-down enable. 0 – Do not stop the oscillator during sleep mode (reset condition). 1 – Stop the 3.6-MHz oscillator during sleep mode.
1	FP	Float PCMCIA controls during sleep mode. This bit determines whether the PCMCIA control signals are driven to a high (negated) state during sleep or not driven (floated). A zero indicates that the pins are driven low. A one indicates that they will be floated. This bit is zero at hardware reset. The PCMCIA signals affected by this bit are: nPOE , nPWE , nPIOW , nPIOR , nPCE<2:1> , nIOIS16 , and nPWAIT . PSKSEL and nPREG are derived from address signals and assume the state of the address bus during sleep.
2	FS	Float static chip selects during sleep mode. This bit determines whether the static chip select control signals are driven to a high during sleep or floated. A zero indicates that the pins are driven low. A one indicates that they will be floated. The static chip select signals affected by this bit are: nCS<3:0> , nOE , and nWE . This bit is zero at hardware reset.
3	FO	Force 32-kHz oscillator enable on. This bit is used to allow software to force the SA-1100 to use the 32-kHz oscillator for internal clocking functions instead of waiting for it to stabilize in the normal way. This function is useful primarily to attain rapid functionality after a "warm" hardware reset when it is known that the oscillator is stable. Use of this bit is intended for test purposes and <i>some</i> customer use in special situations. It should be used with care, however, since setting this bit when the 32-kHz oscillator is not stable will yield unpredictable results.
31..4	—	Reserved.

9.5.7.3 Power Manager PLL Configuration Register (PPCR)

The PPCR contains bits used to configure the core operating frequency generated by the PLL. The following table shows the bit-field definitions for this register. See Chapter 8, “Clocks” for the frequencies generated through settings in this register. Note that the contents of this register are preserved during sleep mode and do not need to be re-initialized after a wake-up event. The PPCR is only cleared upon the assertion of nRESET (hard reset).

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	Reserved											CCF 4	CCF 3	CCF 2	CCF 1	CCF 0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
4-0	CCF<4:0>	Clock speed configuration. See Chapter 8, “Clocks” for the values in this field.
31..5	—	Reserved.

9.5.7.4 Power Manager Wake-Up Enable Register (PWER)

The following table shows the location of all wake-up interrupt enable bits in the PWER. For a GPIO to serve as a wake-up source, it must be programmed as an input in the GPDR. When a fault condition is detected in the VDD_FAULT or BATT_FAULT pins, this register is set to hexadecimal 0000 0003, enabling only GP<1,0> as wake-up sources. This register is also set to this value on hard reset (nRESET asserted). For reserved bits, writes are ignored and reads return zero.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	WE31	Reserved			WE27	WE26	WE25	WE24	WE23	WE22	WE21	WE20	WE19	WE18	WE17	WE16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	WE15	WE14	WE13	WE12	WE11	WE10	WE9	WE8	WE7	WE6	WE5	WE4	WE3	WE2	WE1	WE0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Name	Description
{n}	WE{n}	Sleep wake-up enable n (where n = 0 through 27). 0 – Wake-up due to GPIO<n> edge detect disabled. 1 – Wake-up due to GPIO<n> edge detect enabled.
30..28	—	Reserved.
31	WE31	Sleep wake-up enable 31. 0 – Wake-up due to RTC alarm disabled. 1 – Wake-up due to RTC alarm enabled.

9.5.7.5 Power Manager Sleep Status Register (PSSR)

PSSR contains five status flags. The software sleep status flag is set when sleep mode is entered as a result of the force sleep (FS) control bit being set by the CPU. The battery fault status bit is set any time the BATT_FAULT pin is asserted (even when the SA-1100 is already in sleep mode). The VDD fault status bit is set only when the assertion of the VDD_FAULT pin causes sleep mode invocation (that is, if the force sleep bit is asserted and sleep mode is entered followed by the assertion of the VDD_FAULT pin, the VDD fault status bit is not set). Hardware (power-on) reset clears PSSR, but the sleep mode reset, software reset, and watchdog reset do not affect this register. The peripheral hold and DRAM hold bits indicate that those two interfaces retain the same value as during sleep until these bits are cleared.

The five status flags are cleared when a one is written to them. Writing zero to any status bit has no effect. Reserved bits read as zeros and are unaffected by writes. The following table shows the PSSR.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	Reserved											PH	DH	VFS	BFS	SWS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
0	SS	Software sleep status. 0 – Chip has not been placed in sleep mode by setting the force sleep (FS) control bit since it was last cleared by reset or by the CPU. 1 – Chip was placed in sleep mode by setting the force sleep (FS) control bit.
1	BFS	Battery fault status. 0 – BATT_FAULT pin has not been asserted since it was last cleared by a hardware reset or by the CPU. 1 – BATT_FAULT pin has been asserted.
2	VFS	VDD fault status. 0 – VDD_FAULT pin has not been asserted since it was last cleared by a hardware reset or by the CPU. 1 – VDD_FAULT pin was asserted in run or idle mode and caused the chip to enter sleep mode. Note: This bit will not be set by the assertion of VDD_FAULT while the SA-1100 is in sleep mode.

Bit	Name	Description
3	DH	DRAM control hold. This bit is set upon exit from sleep mode and indicates that the RAS<3:0> and CAS<3:0> continue to be held low and that the DRAMs are still in self-refresh mode. This bit should be cleared by the processor (by writing a one to it) after the DRAM interface has been configured but before any DRAM access is attempted. The RAS and CAS lines are released when this bit is cleared. This bit is cleared on hardware reset.
4	PH	Peripheral control hold. This bit is set upon exit from sleep mode and indicates that the peripheral pins are being held in their sleep state. This bit should be cleared by the processor (by writing a one to it) after the peripheral interfaces have been configured but before they are actually used by the processor.
31..5	—	Reserved.

9.5.7.6 Power Manager Scratch Pad Register (PSPR)

The power manager also contains a 32-bit register to save processor configuration information in any format the user desires. The power manager scratch pad register (PSPR) is a holding register that is powered by the VDDx power supply pins and is never reset (only configured via writes). Any value can be written to it while in run mode. The value remains intact while in sleep mode, and can be read once sleep mode is exited. The user may use the register value to represent processor configuration prior to sleep mode invocation. (The 32 bits can represent encoded configuration information or can act as a pointer to ROM where a configuration table is kept.) The PSPR is a simple read/write register. See the Section 9.5.8, “Power Manager Register Locations” on page 9-40 for its physical address.

9.5.7.7 Power Manager GPIO Sleep State Register (PSSR)

The sleep state register (PSSR) allows the user to select the output state of each GPIO pin when the SA-1100 goes into sleep mode. When a transition to sleep is required (either through software or through the assertion of the BATT_FAULT or VDD_FAULT pins), the contents of the PSSR is loaded into the GPIO output data register. [This register is normally controlled by software through the GPSR (set) and GPCR (clear) registers]. Only pins already configured as outputs will reflect the new state; however, all 28 bits of the output register are loaded. After the SA-1100 reenters the run mode from sleep, these GPIO pins retain their programmed sleep state until changed by writing ones to the GPSR or GPCR registers; question marks indicate that the values are unknown at reset. If a pin direction is switched from an input to an output, the last contents of the register will be driven onto the pin.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	Reserved				SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20	SS19	SS18	SS17	SS16
Reset	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	SS15	SS14	SS13	SS12	SS11	SS10	SS9	SS8	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bit	Name	Description
{n}	SS{n}	Sleep state of GPIO n (where n = 0 through 27) 0 – This pin is driven to a zero during the transition to sleep (if programmed as an output). 1 – This pin is driven to a one during the transition to sleep (if programmed as an output).
31..28	—	Reserved

9.5.7.8 Power Manager Oscillator Status Register (POSR)

The power manager oscillator status register (POSR) is a single-bit, read-only register that contains a status bit indicating whether the 32.768-kHz oscillator is up to speed after a hardware reset. This bit is set after the expiration of a timer that is clocked by a ring oscillator. This bit will be set within 2–10 seconds after the negation of nRESET.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	Reserved															OOK
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
0	OOK	Oscillator OK. This bit is cleared on a hardware reset and set after the 32.768-kHz oscillator has stabilized. This bit is read only.
31..28	—	Reserved.

9.5.8 Power Manager Register Locations

Table 9-4 shows the registers associated with the power manager and the physical addresses used to access them

Table 9-4. Power Manager Register Locations

Address	Name	Description
0h 9002 0000	PMCR	Power manager control register
0h 9002 0004	PSSR	Power manager sleep status register
0h 9002 0008	PSPR	Power manager scratch pad register
0h 9002 000C	PWER	Power manager wake-up enable register
0h 9002 0010	PCFR	Power manager general configuration register
0h 9002 0014	PPCR	Power manager PLL configuration register
0h 9002 0018	PGSR	Power manager GPIO sleep state register
0h 9002 001C	POSR	Power manager oscillator status register