

3.2.4 Vector Summary

Table 3-1 lists byte addresses, and they normally contain branch instructions pointing to the relevant routines. These addresses (except the reset vector) can be changed (to 0xFFFF xxxx) through the vector adjust facility (bit 13, register 1, coprocessor 15). The vector adjust is cleared at reset and cannot modify the reset vector.

Table 3-1. Vector Summary

Address	Exception	Mode on Entry
0x00000000	Reset	Supervisor
0x00000004	Undefined instruction	Undefined
0x00000008	Software interrupt	Supervisor
0x0000000C	Abort (prefetch)	Abort
0x00000010	Abort (data)	Abort
0x00000014	Not used	—
0x00000018	IRQ	IRQ
0x0000001C	FIQ	FIQ

3.2.5 Exception Priorities

When multiple exceptions arise at the same time, a fixed priority system determines the order in which they will be handled:

1. Reset (highest priority)
2. Data abort
3. FIQ
4. IRQ
5. Prefetch abort
6. Undefined instruction, software interrupt (lowest priority)

Note that not all exceptions can occur at once. Undefined instructions and software interrupts are mutually exclusive because they correspond to particular (nonoverlapping) decodings of the current instruction.

If a data abort occurs at the same time as a FIQ, and FIQs are enabled (that is, the F flag in the CPSR is clear), the SA-1100 will enter the data abort handler and then immediately proceed to the FIQ vector. A normal return from FIQ will cause the data abort handler to resume execution. Placing data abort at a higher priority than FIQ is necessary to ensure that the transfer error does not escape detection; the time for this exception entry should be added to worst-case FIQ latency calculations.