

MILLIMETER-WAVE CMOS DEVICE MODELING AND SIMULATION

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ABSTRACT

Challenges for modeling and simulating active and passive 130-nm CMOS devices at mm-wave frequencies (>30 GHz) are discussed. Small-signal lumped circuits with appropriate parasitic elements are used to model the active transistor devices with excellent broadband accuracy. Passive element transmission lines are discussed as generic scalable reactive elements suitable for forming resonant circuits with intrinsic transistor capacitance. The trade-offs between physical and electrical circuit models for the transmission lines are presented. Our approach demonstrates that relatively simple models can be used to accurately predict the small-signal performance of CMOS active and passive devices from dc up to mm-wave frequencies.

1. INTRODUCTION

The rapid scaling of CMOS to shorter channel lengths has enabled circuits to operate well into the millimeter-wave (mm-wave) frequency range [1][2]. The design of circuits at frequencies near the limits of any given technology requires accurate modeling of both the active and passive components. Millimeter-wave modeling of CMOS devices presents several unique challenges due to the low-resistivity silicon substrate, parasitic source, drain, and gate resistances, and the multi-layer dielectric with its relatively high loss tangent. In order to properly account for such limitations, new methodologies must be developed which involve careful modeling at several levels of abstraction, allowing trade-offs between accuracy, flexibility, and simulation speed. The methodology that we have developed to model and simulate both active and passive devices up to 65 GHz will be described along with experimental verification.

2. TYPICAL CMOS PROCESS

One of the most important differences between silicon and compound semiconductor technologies is the lossy nature of the substrate. The silicon substrate of a modern CMOS process has a resistivity of around 10 Ω -cm, whereas a III-

V semi-insulating substrate has a resistivity of around 10^7 – 10^9 Ω -cm and can effectively be treated as an ideal dielectric. The lossy substrate poses problems for both active and passive devices. For transistors, signals which couple to the substrate through the source and drain junction capacitors incur significant losses at mm-wave frequencies. For passive components—inductors, capacitors, and transmission lines—the close proximity of the lossy substrate to the metal conductors lowers the attainable quality-factor (Q) of the passives.

Another important characteristic of a CMOS process is the metallization stack. The gate material for a silicon MOSFET is silicided polysilicon, which has a much higher sheet resistance (~ 10 Ω/\square) than that of the metal used for the gates of GaAs FETs. Modern CMOS technologies have also migrated towards all-copper interconnects. While copper possesses the benefit of a higher conductance than aluminum or gold, the fabrication steps require a uniform density of all metal layers. Thus, floating dummy fill metal must be added to empty areas to increase the local density. Conversely, large areas of metal (e.g., for ground planes) are forced to have slots in order to reduce the density. The slots result in additional conductor loss, while the floating dummy metal can create unwanted and unpredictable coupling if exclusion areas are not defined.

3. TRANSISTOR MODELING

The traditional microwave approach uses measured S-parameter models for the design of small-signal circuits. Although S-parameter models are quite accurate and useful, a lumped small-signal circuit model provides several additional benefits. The small-signal circuit model is supported by all simulators and provides smooth data which results in improved convergence. The circuit model also allows extrapolation to frequencies beyond the measurement capabilities of the test equipment.

The physical layout of a single finger of an NMOS device is shown in Fig. 1, which illustrates the significant high-frequency loss mechanisms. A mm-wave transistor model must account for the series source and drain resistances (R_S , R_D), polysilicon gate resistance (R_G), non-

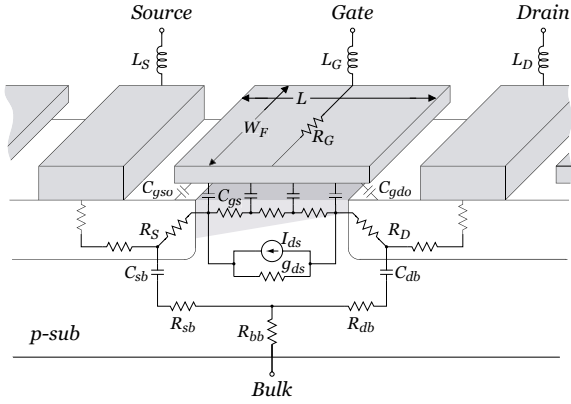


Fig. 1. Physical model for one finger of an NMOS transistor.

quasi-static (NQS) channel resistance (r_{nqs}), and resistive substrate network (R_{sb} , R_{db} , and R_{bb}) [3].

The series source and drain resistances are dominated by the intrinsic spreading resistance in the source-drain extension (SDE) region near the channel. The NQS channel resistance models the effective increase in gate resistance due to the finite channel charging time, and can

be shown to be inversely proportional to g_m . The gate resistance, R_G , accounts for the distributed RC nature of the polysilicon gate, and can be approximated using a single lumped resistor. Additionally, series inductors must be added to all terminals— L_G , L_D , L_S —to properly model the delay effects associated with interconnect wiring.

A test chip consisting of transistors in common-source configuration with W/L ranging from 40/0.13 to 320/0.13 was fabricated in a 130-nm CMOS process. On-wafer mm-wave characterization from 0.04 to 65 GHz was performed on a Cascade Microtech probe station using an Anritsu 37397C VNA and Cascade Microtech GSG coplanar probes. At each bias point, a small-signal lumped model with frequency-independent component values was extracted using a hybrid optimization algorithm in Agilent IC-CAP.

S-parameters for the simulated model and measured data up to 65 GHz are shown in Figs. 2 and 3 for a 100/0.13 NMOS transistor biased at $V_{GS}=0.65$ V and $V_{DS}=1.2$ V. The excellent broadband accuracy of the simulation compared to the measured data is representative of all of our models and verifies that the topology of our small-signal model is correct.

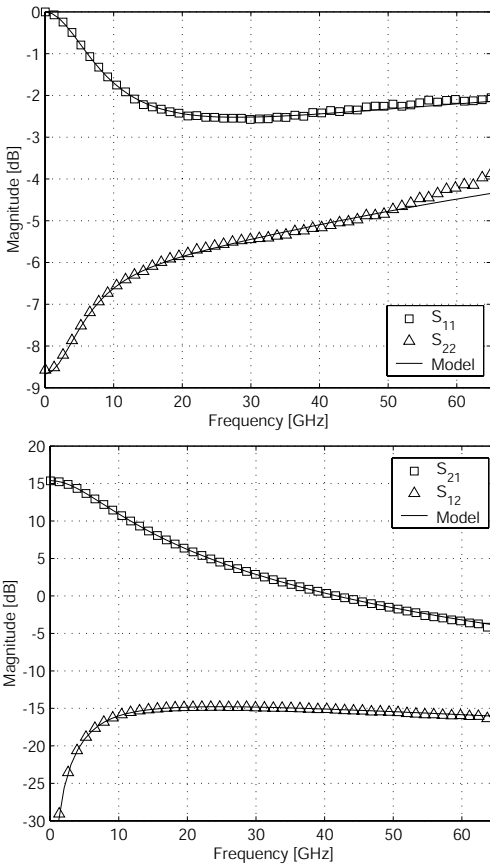


Fig. 2. Measured and modeled S-parameters (magnitude) for a 100/0.13 NMOS transistor ($V_{GS}=0.65$ V, $V_{DS}=1.2$ V).

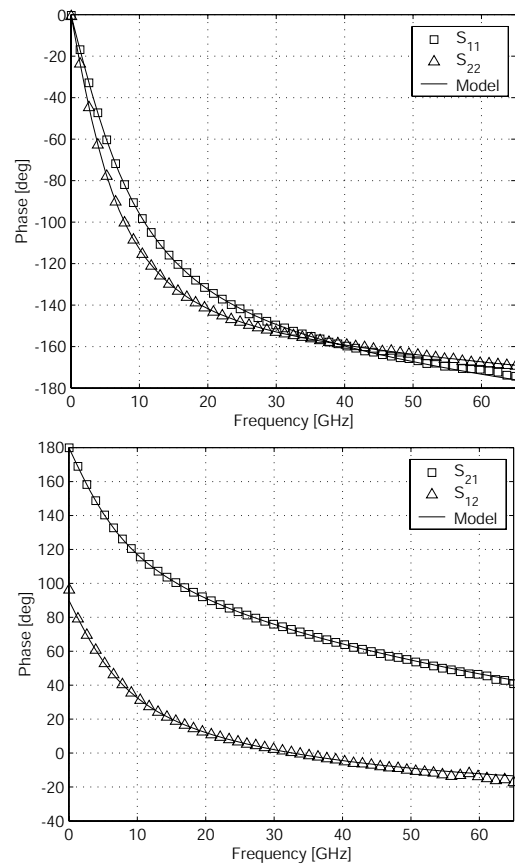


Fig. 3. Measured and modeled S-parameters (phase) for a 100/0.13 NMOS transistor ($V_{GS}=0.65$ V, $V_{DS}=1.2$ V).

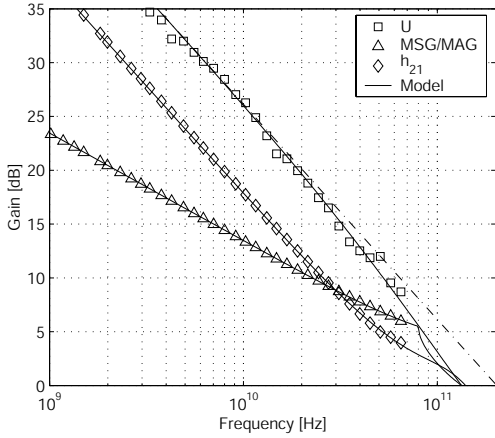


Fig. 4. Measured and modeled gains for a 100/0.13 NMOS transistor ($V_{GS}=0.65$ V, $V_{DS}=1.2$ V).

Furthermore, it also demonstrates that distributed effects and frequency-dependent losses caused by the skin effect can be adequately accounted for using only lumped components with frequency-independent values.

The transistor gains—Mason’s unilateral gain, maximum stable gain (MSG), maximum available gain (MAG), and current gain—for this device are plotted in Fig. 4. The accurate modeling of the unilateral gain is particularly important. Unlike the MSG and current gain, Mason’s unilateral gain is a very strong function of all resistive losses. Therefore, accurately fitting the unilateral gain validates that the important loss mechanisms have been properly modeled. Using the small-signal model, the extrapolated f_{max} is 135 GHz, which is much smaller than the value of 200 GHz if a 20 dB/decade slope is assumed.

4. TRANSMISSION LINE MODELING

For mm-wave circuit design, matching networks and resonators are often realized using transmission lines.

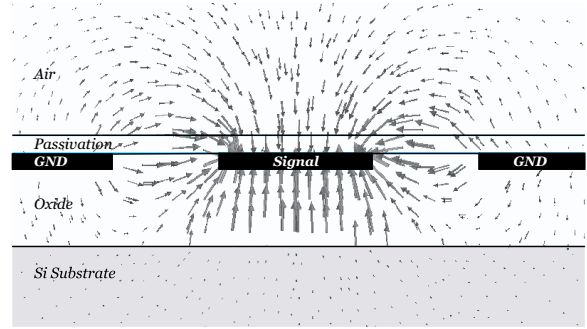


Fig. 5. Cross-section of the electric field distributions from a 3-D EM simulation (HFSS) of a CPW transmission line.

Transmission lines are inherently scalable in length, making them easier to model than lumped passives. Another benefit of using transmission lines is that the well-defined ground return path confines the magnetic and electric fields and significantly reduces any coupling to adjacent structures. Therefore, the lines can be modeled individually without concern that nearby structures will affect the performance characteristics of the line when used in more complex circuits.

The fabricated CMOS test chip also included 1-mm long coplanar waveguide (CPW) transmission lines of different cross-sectional dimensions, producing a large range of characteristic impedances. Equation-based models derived for microwave transmission lines are not applicable for lines integrated on silicon substrates. The models typically assume thin conductors, ground planes which are far from the signal lines, and high-quality dielectrics. The lossy silicon substrate is very close to the signal lines (~ 5 μm) and the metal thickness is on the order of the dimensions of the conductor width and signal-to-ground spacing.

Electromagnetic simulations of the passives based on the physical layout were performed using Ansoft HFSS (Fig. 5). Several simplifications were used to improve simulation time with a small degradation in accuracy. The

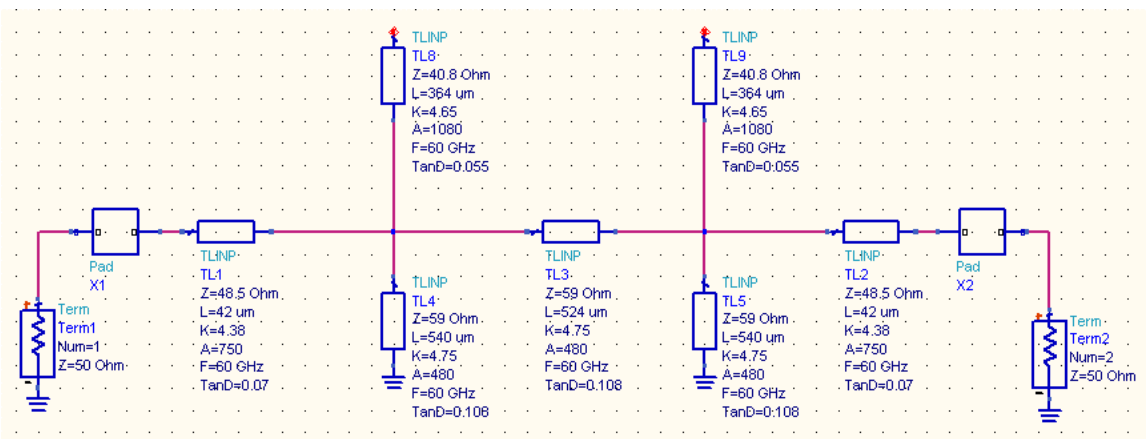


Fig. 6. Schematic of the 30-GHz CPW bandpass filter.

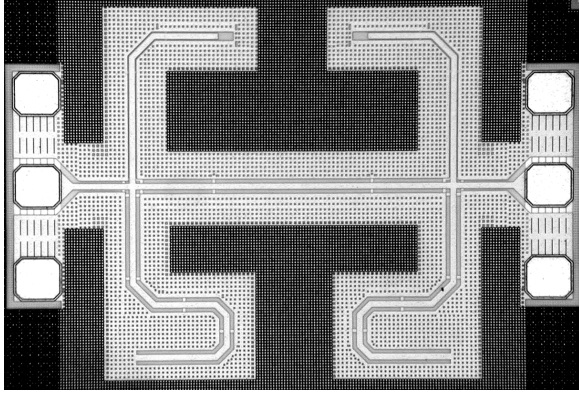


Fig. 7. Chip micrograph of the 30-GHz CPW filter.

silicon substrate is modeled as uniformly doped, and the multilayer dielectrics are modeled with two layers: the oxide and passivation with effective dielectric constants of 4 and 6.3, respectively. Additionally, the dielectric loss tangent, which degrades with frequency, is assumed to be constant. Although 3-D EM simulations enable the characterization of arbitrary passive devices, they suffer from long simulation times (many hours) and the inability to include several poorly characterized effects (substrate doping profile, conductor surface roughness, etc.). Physical EM simulations, therefore, serve as a good verification tool, but are too slow to be used during the design phase.

Another approach is to use electrical models in ADS which capture the high-level behavior of the lines. The model parameters are relatively easy to extract from measured data since only four parameters are required to model the broadband performance of each transmission line: characteristic impedance, effective dielectric constant, attenuation constant, and loss tangent. A first-order frequency-dependent loss model is used. The model assumes that the conductor loss is only caused by the skin effect losses, and the shunt loss is due to a constant loss tangent.

Using simple electrical models has many advantages. The simulation time is very fast, and the models can be easily integrated into commonly-used simulators such as Agilent ADS. Additionally, scalable (in length) models enable the use of powerful optimizers to tune the circuit performance. A broadband pad model was also extracted which consists of a shunt capacitance and series inductance. From our experience, it was not necessary to model the second-order effects such as bends, junctions, end-effects, radiation, and discontinuities to have sufficiently accurate circuit characterization.

To validate our passive models, a 30-GHz bandpass filter, which was composed of series and shunt stubs of the modeled CPW lines, was designed using ADS (Fig. 6). The optimizer was used to determine the line lengths, and

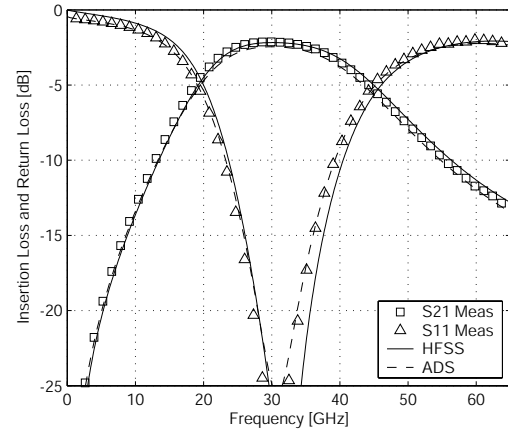


Fig. 8. Measured and simulated results for the 30-GHz CPW filter.

the pads were also included as part of the filter. A die photo of the filter is shown in Fig. 7, and the measured and simulated results for the 30-GHz filter are plotted in Fig. 8, demonstrating excellent broadband agreement for both the physical EM model as well as the simple, scalable electrical models.

5. CONCLUSIONS

We have presented small-signal CMOS transistor models and scalable electrical transmission line models which accurately match measured data up to 65 GHz. Our approach demonstrates that relatively simple models can be used to predict the small-signal performance of CMOS active and passive devices up to mm-wave frequencies. With the available small-signal models, it is now possible to design CMOS circuit blocks, such as amplifiers and oscillators, for mm-wave transceivers.

6. ACKNOWLEDGMENTS

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7. REFERENCES

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