

60 GHz CMOS Radio for Gb/s Wireless LAN

(Invited Paper)

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Abstract—Availability of 7 GHz of unlicensed spectrum in the 60 GHz band motivates the design of a low-cost 60 GHz wireless LAN (WLAN) system. System and circuit barriers to a low cost implementation are discussed and various solutions are proposed.

Index Terms—Wireless LAN (WLAN), mm-wave, wireless LAN, CMOS mm-wave radio.

I. INTRODUCTION

The key motivation for this project is the availability of 7 GHz of unlicensed bandwidth in the 60 GHz spectrum, with numerous obvious advantages and applications. While excessively high path loss at this frequency due to oxygen absorption precludes long-range communication, short-range local area networks actually benefit from the attenuation in providing extra spatial isolation and safety.

Employing inexpensive CMOS technology as opposed to SiGe, GaAs, or InP is a major departure from other efforts. CMOS technology is constantly improving due to a fast growing digital market. Today 130 nm bulk CMOS technology is capable of power gain in the 60 GHz band [3]. Future bulk CMOS at the 65 nm and 45 nm node, and new structures such as the FinFET, are expected to provide even more gain at less power [2].

Many applications require or benefit from high data rates. High quality video signals require data rates exceeding Gb/s. Additionally, sending uncompressed data greatly reduces power overhead for encoding and decoding video. Set-top boxes and digital video cameras are obvious applications for this technology. Automotive collision avoidance radar is another application that is too expensive for mass deployment using today's technology.

In general, though, the need for bandwidth is insatiable, much like the demand for CPU speed, RAM, and external memory. While new spectrum is available in the low-GHz bands, these bands are likely to be overly congested in the near future. Moving up to higher frequency also provides natural isolation from fast digital circuitry typical of today's microprocessors. Lack of package and substrate isolation on-chip plagues many system-on-a-chip (SOC) solutions.

A presumed disadvantage of the 60 GHz radio is the small antenna capture area compared to say 6 GHz WLAN

systems. Since the received power P_r at a distance R is proportional to effective antenna area, and thus to wavelength, a factor of 20 dB loss is expected compared to a 6 GHz system. Assuming simple line of sight communication, the Friis propagation loss is given by

$$\frac{P_r}{P_t} = \frac{D_1 D_2 \lambda^2}{(4\pi R)^2} \propto \left(\frac{\lambda}{R}\right)^2 \quad (1)$$

where the received power P_r normalized to the transmitted power is seen to depend on the TX and RX antenna directivities $D_{1,2}$, distance between RX and TX R , and wavelength λ . While the directivity for a single antenna can be improved, it is more fruitful to increase the directivity by employing an antenna array. The array provides extra diversity, automatic spatial power combining, and electronic beam steering capability. Therefore it is in fact advantageous to move to a higher frequency, since the constant is antenna size, and the antenna array gain actually improves with frequency.

II. RADIO ARCHITECTURE

A. Antenna Array

A generic adaptive beam-forming multiple antenna radio system is shown in Fig. 1. Antenna elements are small enough to be directly integrated into the package. Beam forming improves the antenna gain while also providing spatial diversity and thus resilience to multi-path fading. The main benefit of the multi-antenna architecture used here is the increased gain that the directional antenna array pattern provides. This gain is needed in order to support data rates approaching 1 Gb/s at typical indoor distances. Additionally, the directive antenna pattern improves the channel multipath profile; by limiting the spatial extent of the antenna patterns to the dominant transmission path, the delay spread and Rician K-factor of an indoor wireless channel can be significantly improved [4].

Key elements of an antenna array are the RF phase shifters and voltage-controlled attenuators. An approach that eliminates the need for the RF phase shifters is to generate and process N IF streams appropriately conditioned to drive and receive signals from the antenna array. This is preferable to a similar baseband scheme due to

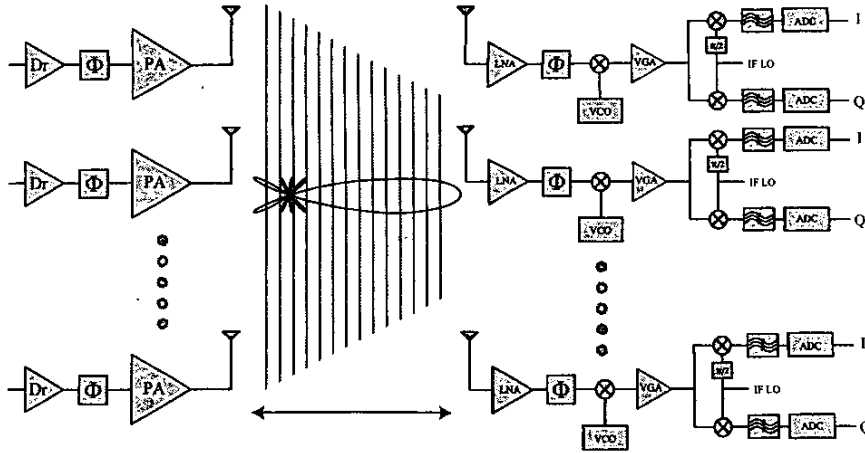


Fig. 1. A multiple antenna transceiver architecture employing antenna steering for maximum gain.

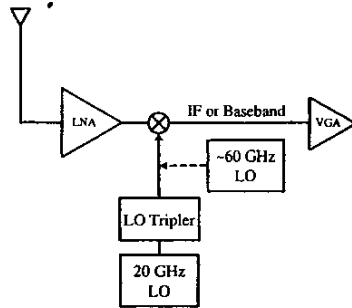


Fig. 2. A 60 GHz radio architecture based on one conversion to an IF of 5 GHz or directly to baseband.

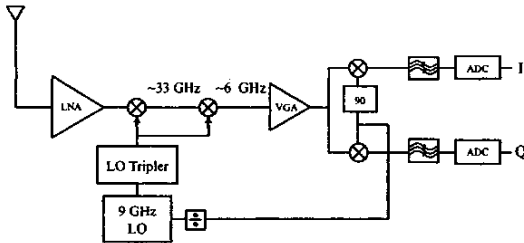


Fig. 3. A multi-stage conversion architecture relaxes LO and frequency synthesizer design.

the high data rate. Alternatively, the phase shifters and attenuators can be done at RF. We have found that the need for high accuracy phase shifters and attenuators is greatly relaxed if one is only concerned with the peak in the antenna directivity.

B. Transceiver Architecture

Two simple receiver architectures for the 60 GHz radio are shown in Fig. 2 and Fig. 3. In the first architecture,

the RF signal is directly down-converted to 5 GHz (or baseband) in one step. This requires a high-frequency LO to operate near 60 GHz. While VCO design is not a major impediment at this frequency, a synthesizer would require frequency dividers to operate at this high frequency. Injection locking can be used to relax the power consumption of dividers [5]. Alternatively, the 60 GHz LO signal can be obtained by a 20 GHz LO and a frequency tripler. This approach has been shown to be effective for obtaining a 17 GHz IQ LO [6]. The second approach, shown in Fig. 3, uses double conversion. The 9 GHz LO is tripled and used to down-convert from 60 GHz to 33 GHz, and then again down to an IF of around 6 GHz. It is interesting to note that image-reject mixers is not strictly needed for the 27 GHz LO since the image frequency is sufficiently far to be easily low-pass filtered. Since 60 GHz power gain comes at a DC power consumption premium, only enough gain is used to overcome the noise of subsequent stages. In all three architectures, most gain will therefore come from IF and baseband stages.

C. Packaging

We intend to integrate N (about 10) transceivers in an LTCC substrate. The LTCC substrate has low loss, and flip-chip bonding will minimize the parasitic inductances. MEMS technology offers another attractive alternative to the package. Using a low-temperature MEMS back-end process such as demonstrated by [7], antenna elements can be introduced directly on top of the transceiver. Each antenna element occupies an area of 4mm^2 , commensurate with the transceiver size. To eliminate the loss associated with the proximity of the Si substrate, a hinge can physically move the antenna perpendicular to the substrate. Otherwise a null can be inserted in the array to avoid irradiating the substrate.

III. KEY RF BUILDING BLOCKS

Since N transceivers are operating in parallel, RF power consumption is key. To realize gain close to the limits of process technology, though, requires relatively high power consumption. The power is expected to drop when employing 90 nm and beyond technology. Due to the lack of accurate models for active and passive elements in CMOS technology at 60 GHz, a conservative design approach was favored at the early stage.

Simple gain stages consisting of NMOS common-source cascode amplifiers are used extensively for power gain. Inductive degeneration, common in low-GHz design, is avoided to maximize the gain. Transmission lines are used extensively to realize small inductive reactances in matching networks. The design of proper coupling and bypass capacitors are non-trivial at these frequencies due to self-resonance. If a bypass capacitor is oversized or designed incorrectly, it may self-resonate below 60 GHz and produce unwanted oscillations. Finger MIM capacitors are preferred to parallel plate MIM capacitors for compatibility with a generic CMOS process. Furthermore, the MIM capacitor dielectric has not been characterized at 60 GHz and represents a potential risk in the design.

The Gilbert cell mixer is the workhorse of many low-GHz designs. Due to the operation close to the limits of the process, simpler architectures may be preferred. Microwave diode ring mixers reign supreme in traditional microwave design. Low loss diodes are not available in a traditional digital CMOS process and so other alternatives such as dual gate mixers or single transistor mixers are explored. These architectures offer conversion gain, which is desirable for rejecting the noise of the proceeding RF stages.

The pseudo dual-gate mixer is a cascode device. The gate of transistor is driven by an RF signal where its $g_m(t)$ is modulated by the LO signal applied to gate of the cascode. This mixer is compact and provides a degree of isolation between RF and LO. The single transistor mixer is even simpler, but requires a hybrid coupler to combine an LO and RF signal. The transistor non-linearity produces the desired mixing product. Due to the high frequency of operation, though, the hybrid can be easily and necessarily integrated on-chip.

CMOS VCOs have already been demonstrated in CMOS operating at 60 GHz [1]. Relatively high Q (about 20) LC or transmission line resonators have been measured in these frequency bands. The achievable phase noise is around -85 dBc/Hz at a 100 kHz offset. Since the VCO is a shared block among the parallel transceiver sections, DC power consumption is not the primary concern. As already discussed, generation of a stable frequency reference is a concern and may dictate a lower frequency LO.

The need for a power amplifier is ameliorated by the

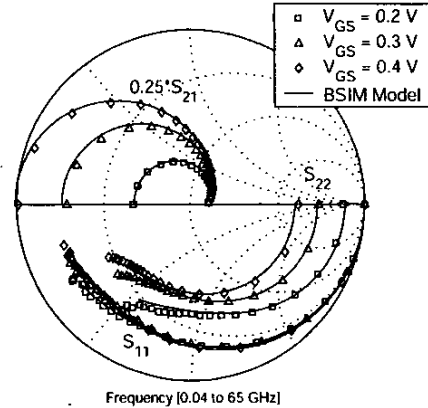


Fig. 4. Modified BSIM3 model with enhanced parasitics is capable of predicting RF small signal and large signal performance up to 60 GHz.

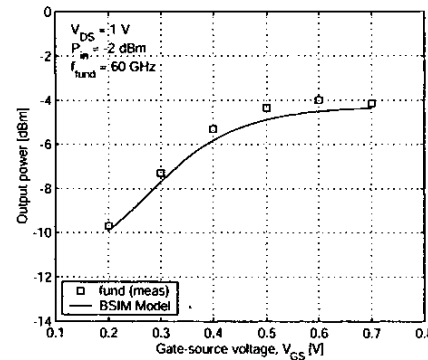


Fig. 5. The gain compression of a single transistor at 60 GHz.

spatial power combining shown in Fig. 1. To transmit 100mW, for instance, 10 amplifiers need only deliver 10mW. The reduced power eases matching network design, a traditional source of loss in an integrated power amplifier, and spatial power combining eliminates the need for power combining off-chip. Since power combiners are generally lossy and bulky, this greatly benefits the design and integration of the overall system. If needed, coarse power control is simply achieved by turning off parallel stages.

IV. MM-WAVE ACTIVE AND PASSIVE ELEMENTS

Scattering parameters of single transistor and cascode device structures are carefully measured from DC to 65 GHz. Custom layout transistors are fitted to models. It is found that a modified lumped circuit sufficiently models small and large signal performance up to 65 GHz [3]. In Fig. 4, a modified BSIM3 model has been used to model an 80 finger device. S-parameters show a good match over the entire band of interest. A plot of the transistor gain

compression at 60 GHz is shown in Fig. 5. It's important to note that the DC non-linearity is used to predict high frequency performance. This greatly simplifies extraction of the compact model parameters.

Transmission lines are used extensively in the design, as discussed in [3]. Co-planar lines are preferred over microstrip lines due to higher obtainable inductive quality factors. This is important since transmission lines are used extensively to resonate MOS capacitors. Furthermore, since lateral dimensions are determined by lithography, the characteristic impedance of the co-planar line is more predictable and constant over process. Inductive quality factors as high as 19 have been measured for coplanar lines. The inherent two-dimensional layout and scalability of transmission lines also simplifies simulation and compact modeling.

For more compact layouts, ring inductor based resonators are promising. The quality factor of a 150 pH ring inductor resonating with MIM capacitors has been measured. The resonator occupies an area of $150^2 \mu\text{m}^2$ and has a loaded measured quality factor over 20.

V. BASEBAND AND SYSTEM ARCHITECTURE

The circuits described above are to be utilized in the design of a 60 GHz indoor wireless transceiver capable of Gb/s data rates. In high data rate systems, the choice of baseband architecture can have a large impact on the overall system complexity and power consumption of the mobile transceiver. In typical "mostly digital" wireless receivers or transmitters, high resolution interface circuitry (ADCs and DACs) are required to convert the signal waveform between the analog and digital domain so that the subsequent or preceding digital processing is not limited by accuracy of these interface circuits. In multiple-antenna systems, where there may be several instantiations of the baseband circuitry, the aggregate power consumed by these high-speed, high-resolution interface circuits may become prohibitively large.

However, if more of the signal processing is pushed into the analog domain, the resolution requirements of the interface circuitry drops significantly. This hybrid or "mostly analog" approach has been frequently used in high-speed serial/deserializer (SerDes) architectures, where baud rates on the order of several Gb/s prohibit high-speed, high-resolution converter circuitry [8]. Equalization and timing and carrier synchronization can be performed using a mixed-signal approach: maximum-likelihood estimation of the various parameter errors can be performed in the digital domain, where robust and powerful algorithms can be performed in low-power digital CMOS architectures. These parameter errors are corrected in the analog domain, where simple high-speed analog circuits can properly condition the analog circuit prior to analog-to-digital conversion. Since the analog signal is properly conditioned before

being converted, the resolution requirement of ADC is reduced, resulting in significant power savings. Applying these techniques to a high-speed multi-antenna system can dramatically reduce the overall power consumption, as the additional overhead in analog signal processing is small when compared to the savings in converter complexity.

VI. CONCLUSION

The feasibility of a CMOS wireless transceiver capable of 60 GHz operation has been demonstrated. By carefully developing passive and active device models from measured data, key RF building blocks such as amplifiers, mixers, and oscillators can be realized. By employing multiple antennas in a dynamic beam steering configuration, the extra path loss at 60 GHz can be tolerated. A mixed-signal "mostly analog" baseband architecture is also key in reducing the power consumption and dynamic range requirements of the ADCs.

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REFERENCES

- [1] M. Tiebout, et al., "A 1V 51 GHz fully-integrated VCO in $0.12\mu\text{m}$ CMOS," *IEEE Int. Solid-State Circuits Conf. Dig. Tech.*, pp. 238-239, Feb. 2002.
- [2] D. Hisamoto, W.-C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T.-J. King, J. Bokor, and C. Hu, "A folded-channel MOSFET for deep-sub-tenth micron era," *Int. Electron Devices Mtg.*, San Francisco, CA, December 1998.
- [3] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Design of CMOS for 60 GHz applications," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2004.
- [4] M. R. A. Williamson, G.E.; Nix, A.R., "Investigating the effects of antenna directivity on wireless indoor communication at 60 GHz," *The 8th IEEE International Symposium on Personal, Indoor and Mobile Radio Communications*, 1997, vol. 2, pp. 635-639.
- [5] H. Rategh, H. Samavati and T. Lee, "A CMOS frequency synthesizer with an injection-locked frequency divider for a 5 GHz wireless LAN receiver," *IEEE J. Solid-State Circuits*, vol. 35, pp. 780-787, May 2000.
- [6] D.K. Ma, J. Long and D. Hareme, "A subharmonically-injected quadrature LO generator for 17 GHz WLAN applications", *CICC 2003*.
- [7] A. E. Franke, Y. Jiao, M. T. Wu, T.-J. King and R. T. Howe, "Post-CMOS modular integration of poly-SiGe microstructures using poly-Ge sacrificial layers," *Solid-State Sensor and Actuator Workshop Technical Digest*, pp. 18-21, June 2000.
- [8] J. Zerbe, et al, "Equalization and clock recovery for a 2.5-10Gb/s 2-PAM/4-PAM backplane transceiver cell," *IEEE Int. Solid-State Circuits Conf. Dig. Tech.*, pp. 80-81, Feb. 2003.