

Large-Signal Millimeter-Wave CMOS Modeling with BSIM3

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Abstract — A large-signal modeling methodology based upon a modified BSIM3v3 transistor model is presented which targets mm-wave CMOS applications. The effect of parasitics on the high-frequency operation of CMOS transistors is discussed, and a standard intrinsic BSIM3v3 model card is augmented with lumped elements to model these effects. Core BSIM parameters are extracted to match the measured dc I-V curves of a fabricated common-source NMOS transistor. Measured S-parameters are used to extract external parasitic component values to obtain a bias-dependent small-signal mm-wave frequency fit up to 65 GHz. Large-signal mm-wave accuracy of the model is verified by measuring the output harmonics power under large-signal excitation. Comparisons of measurements with the simulations show good agreement up to 60 GHz.

Index Terms — BSIM3, CMOS large-signal model, harmonic power, mm-wave CMOS modeling.

I. INTRODUCTION

The increasing popularity of the 24-GHz ISM and 60-GHz unlicensed bands for wireless communications combined with CMOS scaling yielding faster devices present a great opportunity for using mainstream CMOS technology for millimeter-wave (mm-wave) radios. A low-noise amplifier and mixer front-end operating at 24 GHz and implemented in 0.18- μm CMOS technology has been demonstrated [1]. Moreover, the results in [2] indicate that a 0.13- μm NMOS transistor can achieve a peak f_{max} of 135 GHz, and by careful design and layout of the active and passive components, a standard digital 0.13- μm CMOS technology is capable of 60-GHz operation.

With the operating frequency approaching the limits of CMOS technology, modeling accuracy becomes more critical as the performance margins shrink. Recent results have demonstrated highly accurate, broadband small-signal CMOS models up to 65 GHz for fixed bias points [2]. Although ac models are often sufficient for the design of linear circuit blocks, the optimization of nonlinear circuits such as mixers, power amplifiers, oscillators, and frequency multipliers, requires precise knowledge of the nonlinear characteristics of the active devices over a wide range of operation.

Large-signal device models have evolved into two basic categories: table-based [4] and physical [5][6]. At mm-wave frequencies, GaAs FET models commonly employ table-based models derived from bias-dependent linear

measurements. The large-signal accuracy of table-based models is limited by the existence of discontinuities in the model elements and nonlinearities in their interpolation due to imperfect measurement data [7]. Recent efforts to model the large-signal distortion performance of CMOS transistors with compact models have provided accurate results, but have been verified only at frequencies below 2 GHz [6][8].

In this paper, we introduce an extension to the standard BSIM3 modeling procedure, and provide experimental validation of small-signal and large-signal accuracy up to 65 GHz.

II. MODELING METHODOLOGY

The proposed modeling methodology is based on the quasi-static assumption that the mm-wave large-signal performance of a transistor is primarily governed by its dc nonlinearities. Furthermore, the dynamic performance can be modeled with the addition of extrinsic parasitics to capture loss and inductive effects, which become particularly important at mm-wave frequencies.

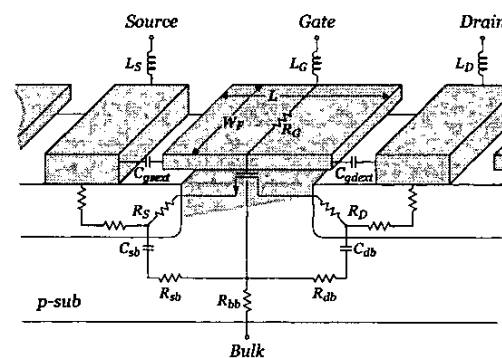


Fig. 1. Simplified physical model for one finger of an NMOS device with external parasitics.

The physical layout of a single finger of an NMOS device is shown in Fig. 1, which illustrates the significant high-frequency extrinsic parasitics. A mm-wave transistor model must account for the series source and drain resistances (R_S , R_D), polysilicon gate resistance (R_G), and resistive substrate network (R_{sb} , R_{db} , and R_{bb}) [3]. The

proposed modeling methodology uses a core BSIM model for the intrinsic transistor, augmented with extrinsic parasitics as depicted in Fig. 2.

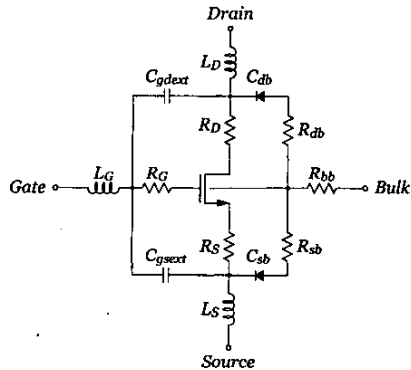


Fig. 2. BSIM3 core model with extrinsic parasitics.

The series source and drain resistances are dominated by the intrinsic spreading resistance in the source-drain extension (SDE) region near the channel. The gate resistance, R_G , accounts for the distributed RC nature of the polysilicon gate, and can be approximated using a single lumped resistor. Additionally, series inductors must be added to all terminals— L_G , L_D , L_S —to properly model the delay effects associated with interconnect wiring. Layout-dependent interconnect capacitances are also added around the intrinsic device, and junction diodes account for the voltage-dependence of C_{db} and C_{sb} .

III. MODEL EXTRACTION

A die micrograph of an $80 \times 1 \mu\text{m} / 0.13 \mu\text{m}$ NMOS transistor, optimized for operation at mm-wave frequencies and fabricated on a standard $0.13 \mu\text{m}$ CMOS process, is shown in Fig. 3. De-embedding structures were used to remove the effects of the pads from the small-signal device characterization.

For dc large-signal characterization, I-V measurements

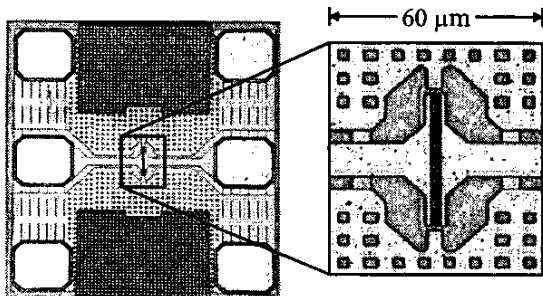


Fig. 3. Micrograph of the $80 \times 1 \mu\text{m} / 0.13 \mu\text{m}$ NMOS device.

were used to extract the core BSIM parameters of the fabricated common-source NMOS. As shown in Figs. 4 and 5, a good agreement between measured and modeled dc curves can be achieved for this device.

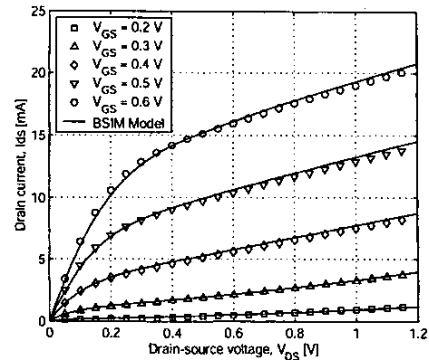


Fig. 4. Measured and modeled I_{DS} vs. V_{DS} .

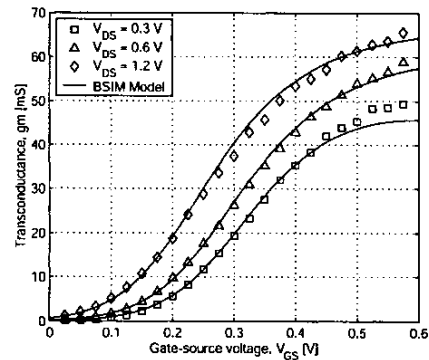


Fig. 5. Measured and modeled g_m vs. V_{GS} .

Next, over a wide bias range, extensive on-wafer S-parameter measurements to 65 GHz were performed on a Cascade Microtech probe station using an Anritsu 37397C VNA and Cascade Microtech GSG coplanar probes. The external parasitic component values for the model were extracted using a hybrid optimization algorithm in Agilent IC-CAP. S-parameters for the simulated model and measured data up to 65 GHz are shown in Fig. 6 for a typical bias sweep over V_{GS} for the de-embedded transistor. The broadband accuracy of the model verifies that using lumped parasitics (Fig. 2) is suitable well into the mm-wave region.

IV. LARGE-SIGNAL MEASUREMENT SETUP

The nonlinear model described in Section II needs experimental verification. Two common approaches to characterize transistor mm-wave nonlinearity are with

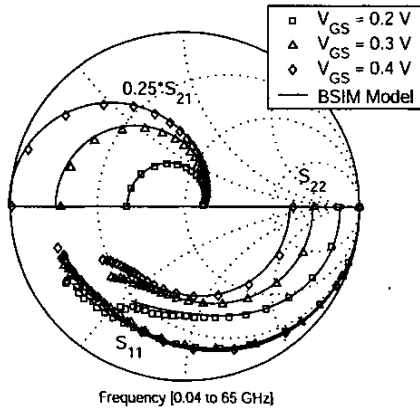


Fig. 6. Measured and modeled S-parameters for $V_{DS} = 1.2$ V and $V_{GS} = 0.2-0.4$ V.

mm-wave load-pull measurements and power spectrum analysis [9]. While the former requires automated tuners, the latter, which was chosen in this work, can be performed with only a synthesizer, VNA, and power meter (Fig. 7). The fabricated device is driven over a wide range of input power and bias conditions, while the output powers at the fundamental and harmonic frequencies are measured.

In the harmonics power measurement setup of Fig. 7, the VNA is configured as a receiver in the Set-On mode. In this mode of operation, the source lock circuitry of the 37397C is completely bypassed which allows all of the 37397C samplers to operate over their full dynamic range. The 65-GHz synthesizer and 37397C are locked to the same 10-MHz reference, enabling coherent reception at the harmonic frequencies. A 65-GHz high dynamic-range power sensor is used to de-embed the insertion loss of the cables, probes, adaptors, etc. from the measurements. Port2 of the VNA requires a 10-dB attenuator to avoid compression when the fundamental power is strong, thus limiting the sensitivity of the power measurement at 60

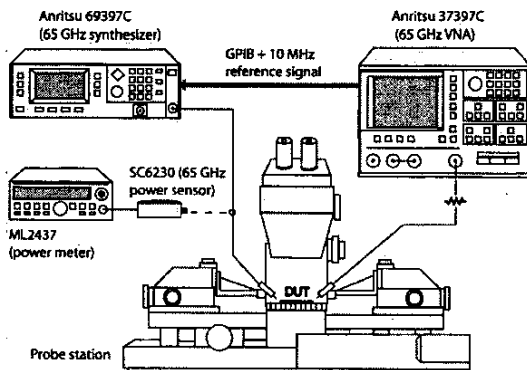


Fig. 7. Test setup for mm-wave harmonics measurements.

GHz to approximately -35 dBm.

V. MEASURED AND SIMULATED RESULTS

A. Bias-Dependent Large-Signal Verification

The proposed BSIM model was implemented in Agilent EEsof ADS, and the harmonic balance simulator was used to predict the large-signal behavior. Fig. 8 shows the measured and modeled fundamental, second, and third harmonics at the output when the device is driven by a 20-GHz 0-dBm signal with a bias of $V_{DS} = 1$ V and variable V_{GS} . The output powers at the fundamental and second harmonics agree very well, whereas the agreement at the third harmonic is reasonable, but not as good. The measurement of the third harmonic for $V_{GS} > 0.4$ V is limited due to the dynamic range of the VNA samplers at 60 GHz.

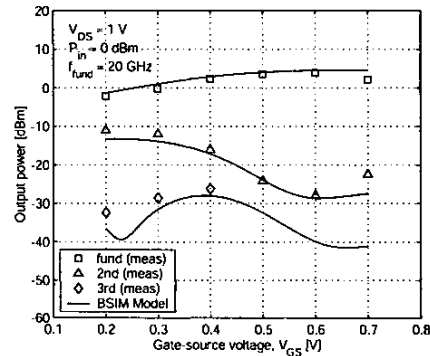


Fig. 8. Fundamental, second, and third harmonics vs. the gate bias (V_{GS}) for $V_{DS} = 1$ V, $P_{in} = 0$ dBm, $f_{fund} = 20$ GHz.

Similar experiments were performed at a different input power (-2 dBm) and signal frequency (30 GHz). Fig. 9 shows the measured and modeled fundamental and second

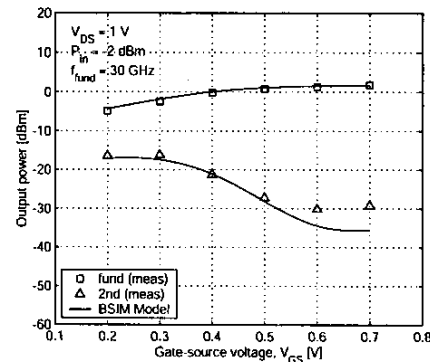


Fig. 9. Fundamental and second harmonic vs. the gate bias (V_{GS}) for $V_{DS} = 1$ V, $P_{in} = -2$ dBm, $f_{fund} = 30$ GHz.

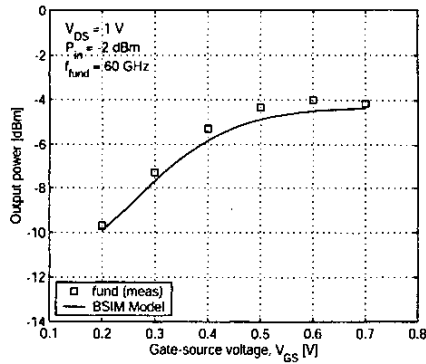


Fig. 10. Large-signal gain vs. gate bias (V_{GS}) for $V_{DS} = 1$ V, $P_{in} = -2$ dBm, $f_{fund} = 60$ GHz.

harmonics of the output signal for the same bias conditions. Good agreement is observed at both the fundamental and second harmonic. Since the second harmonic at 60 GHz is strong, it is within the dynamic range of the measurement setup.

Fig. 10 displays the measured and modeled 60-GHz large-signal amplification characteristics of the device. The model closely predicts the fundamental output power for the device over a large bias range from weak inversion to very strong inversion.

B. Class B Operation

Many mm-wave circuits, such as mixers and frequency multipliers, operate by exploiting the strong nonlinearity of transistors biased near the threshold voltage, effectively using the device as a rectifier. To determine the accuracy of the model for these applications, the transistor was biased at constant $V_{GS} = 0.2$ V, and the input power was swept from $P_{in} = -3$ dBm to $+3$ dBm at a fundamental of 30 GHz. The results shown in Fig. 11 show that the extended BSIM model provides good accuracy for class B operation over a wide range of input signal power.

VI. CONCLUSION

This paper presents a modeling methodology in which an extended BSIM3v3 model is used to accurately predict the small-signal behavior of an NMOS device well into the mm-wave region through careful modeling and extraction of the parasitic elements. Furthermore, the results validate that with accurate dc nonlinearity fitting, the model can predict the harmonic distortion behavior of a device up to 60 GHz. The ability to model the strongly nonlinear case of class B operation is also verified, which suggests that the model is viable for use in the design of nonlinear mm-

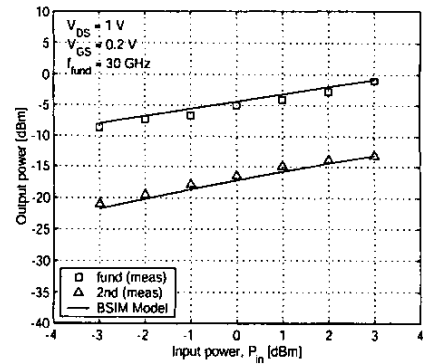


Fig. 11. Class B power sweep curves.

wave blocks such as mixers, power amplifiers, and frequency multipliers.

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