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Low-power Multimedia Wireless Communication Systems

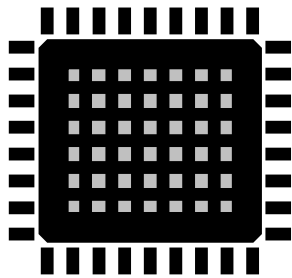
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URL://uivlsi.csl.uiuc.edu/~vips/

Trends and Problems in Integrated Circuits

(Source: Semiconductor Industry Association 1997 Roadmap)

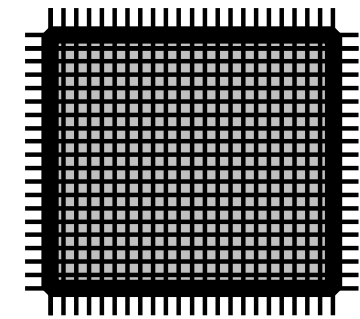
Current day Integrated Circuit



0.2 micron
3.7M/sq.cm
750 MHz
250 MHz
1.8-2.5V
70 Watts
1.2 Watts
0.5-0.75 micron

FEATURE SIZE
DENSITY
ON-CHIP CLOCK
OFF-CHIP CLOCK
SUPPLY VOLTAGE
POWER (HIGH PERF.)
POWER (MOBILE)
WIRE PITCH

Integrated Circuit in 2012*



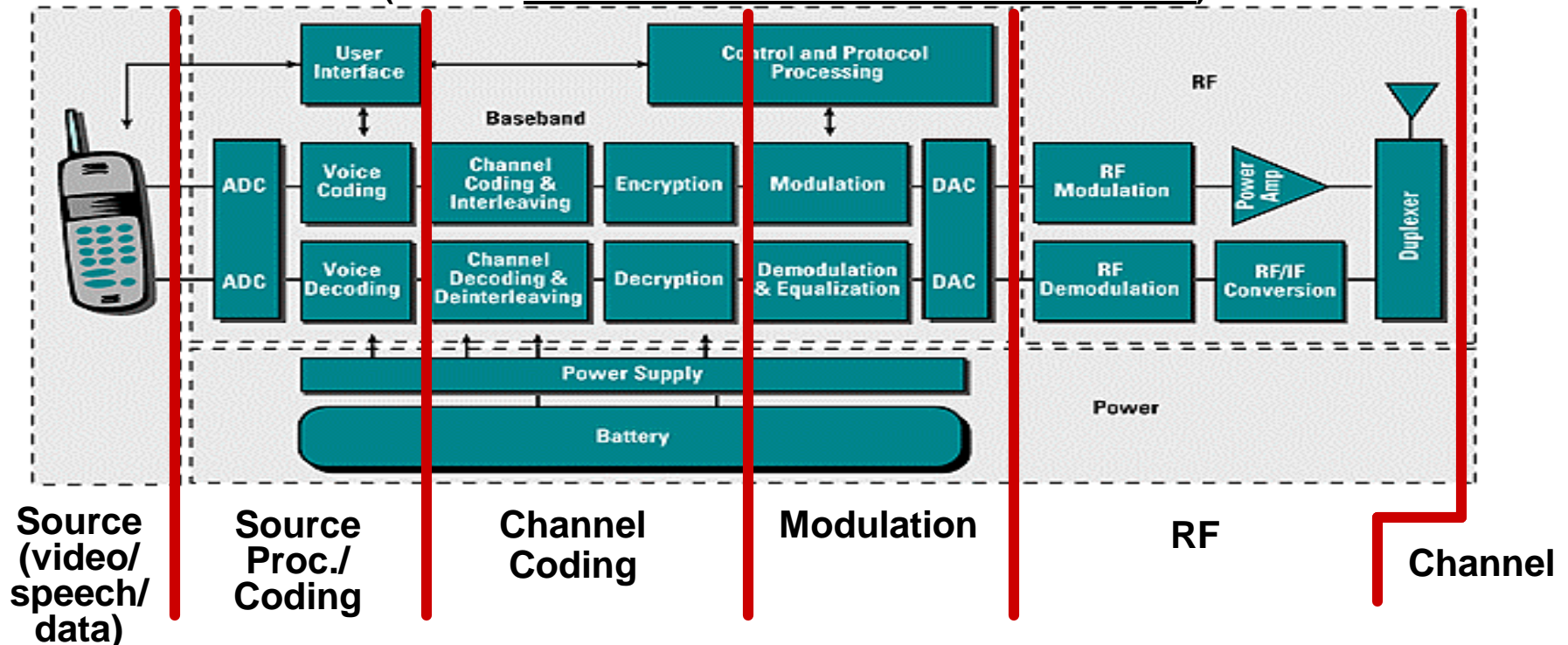
0.035 micron
180M/sq.cm
10 GHz
1.54 GHz
0.5-0.6V
175 Watts
3.2 Watts
0.1-0.15 micron

- Problems (due to Systems-on-a-chip in deep submicron)
 - Time-to-market/Design productivity vs. Design complexity => Solutions: Design reuse via Intellectual Property; Design exploration; H/S codesign, **Reconfiguration**
 - Reliability: noise, signal integrity, process variations => Solutions: noise analysis, smart place&route, **noise-tolerance**
 - Design efficiency: **low-power and high-speed techniques & bounds**



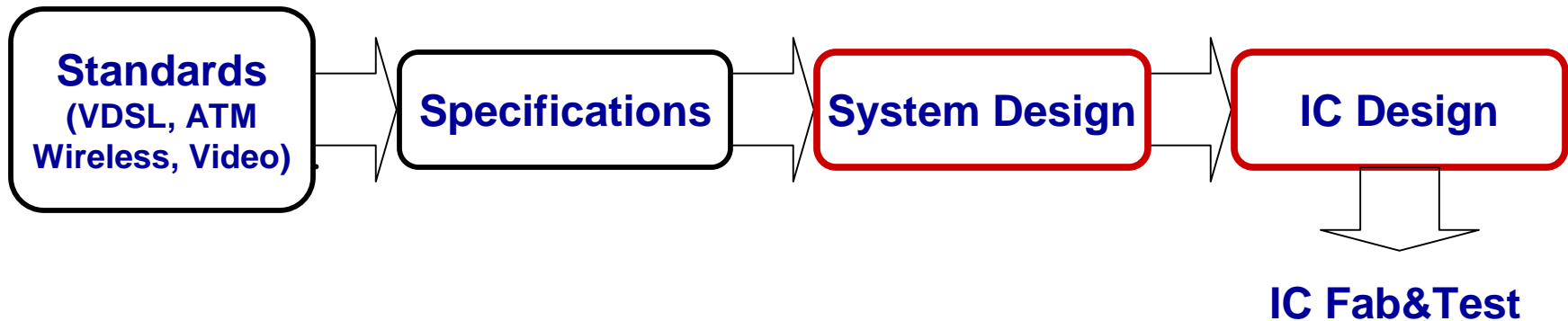
Integrated Multimedia Communication Systems

(Source: www.ti.com/sc/docs/wireless/97/issues.htm)



- Additional Problems:
 - mixed-signal issues: coupling, low-voltage analog, etc.
- Additional Solutions: DSP and communication theory; joint source-channel coding, signal-adapted DSP, multiresolution DSP; well-defined **system/algorithm design**

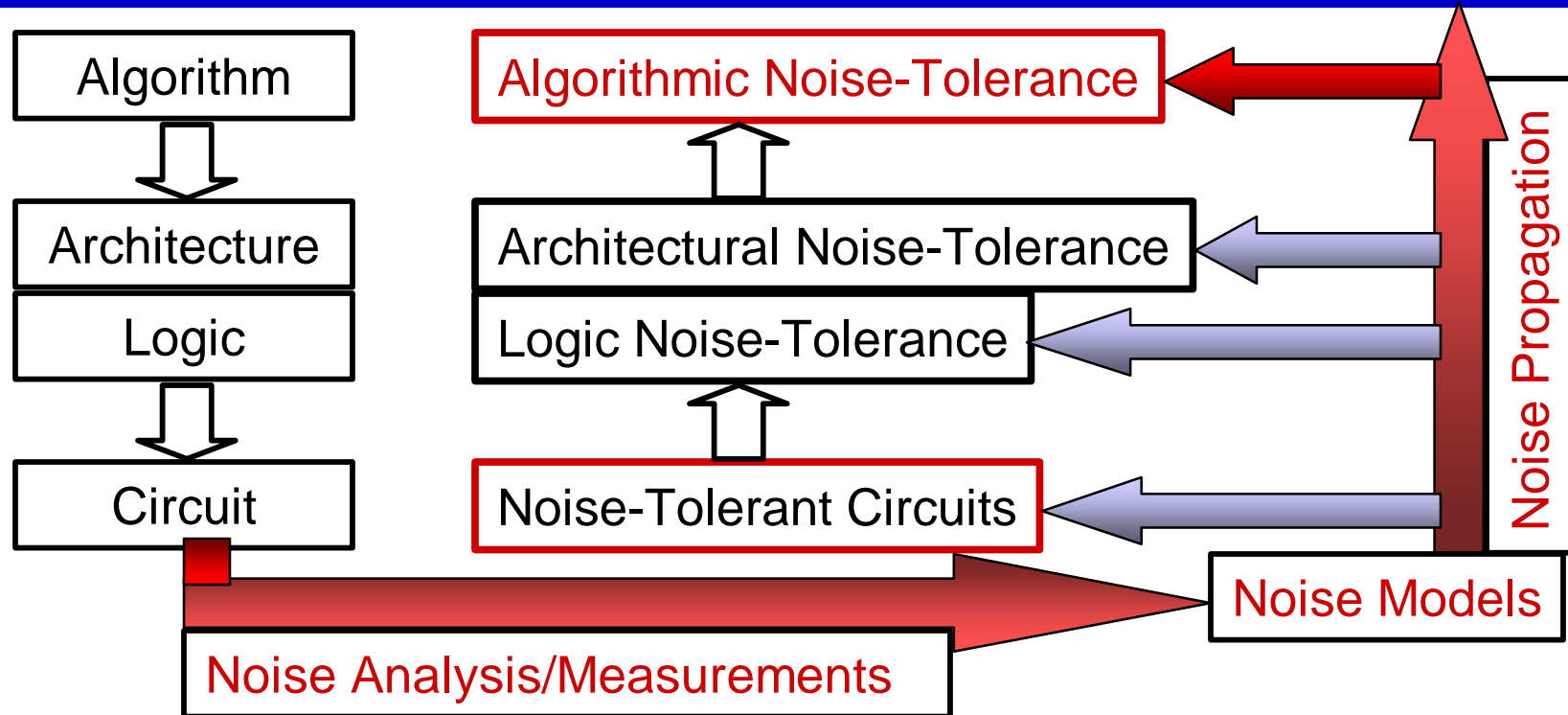
Multimedia Communication System Design



- Projects:
 - Wireline system design: ATM-LAN, VDSL, cable modem (Goel, Hegde, Tschanz)
 - Wireless system design: (Wang)
 - Hermitian decoder ASIC (Profs. Blahut and Kotter, Ashbrook, Feng)
 - Low-power transforms and synthesis: (Profs. Hajj and Najm, Ramprasad, Hegde)



Noise-tolerant VLSI

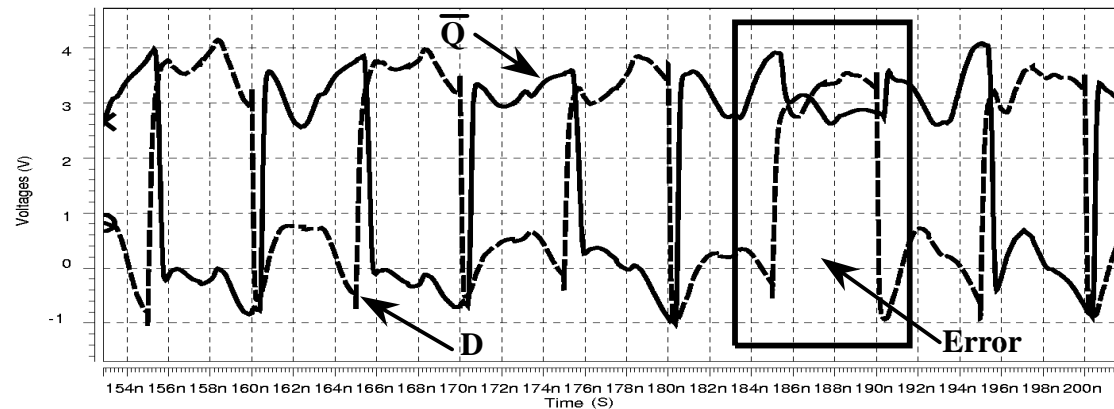
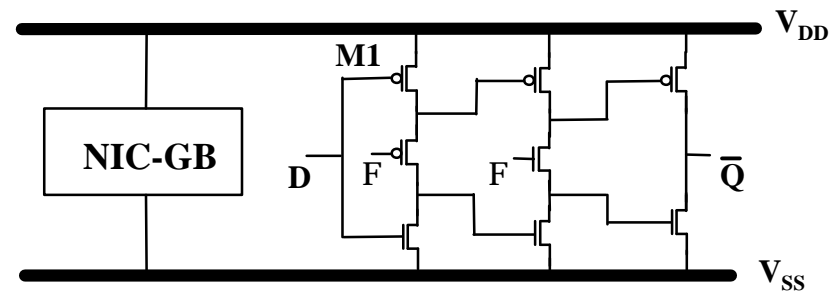


- Projects:
 - Algorithmic noise-tolerance (Hegde, Wang)
 - Noise-tolerant circuits (Wang, Ganesh)
 - Noise-tolerant distributed arithmetic filters (Anders)

Deep Submicron (DSM) Noise

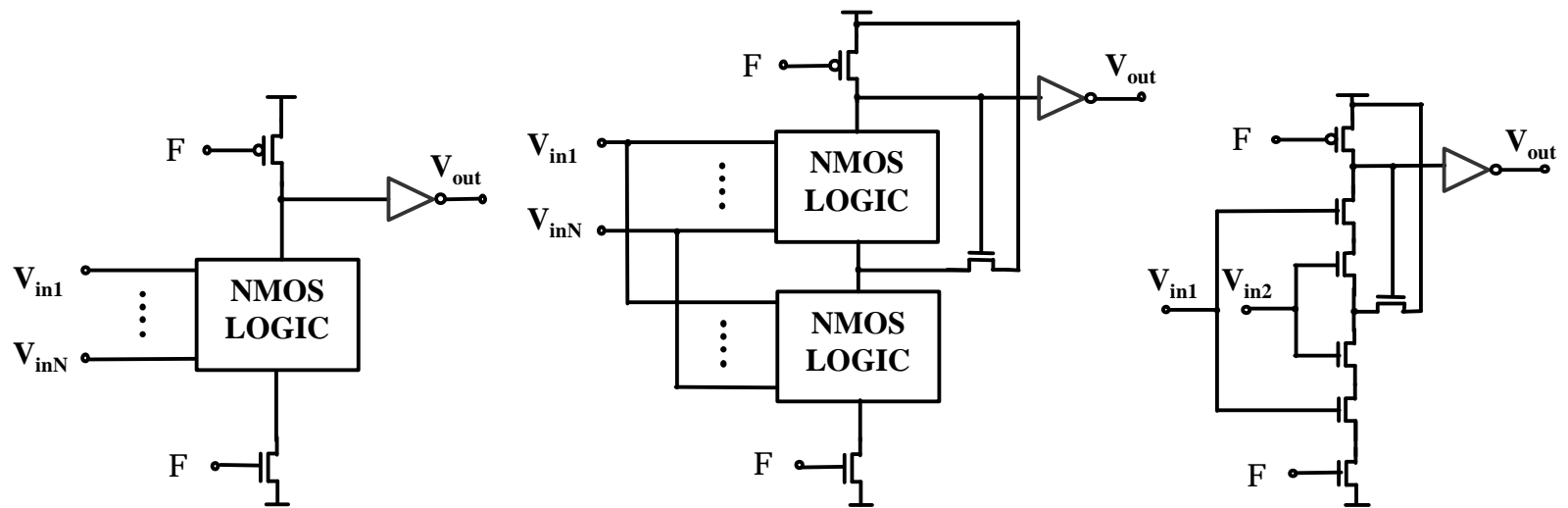
Noise Sources:

- Ground bounce
- IR drop
- Crosstalk
- Charge sharing
- Charge leakage
- Process variations
- Alpha particles
- Electro-magnetic radiation



Noise Problems: aggressive architectural (deep pipelining) and circuit (dynamic, low-voltage) styles.

Mirror Technique For Dynamic Circuit



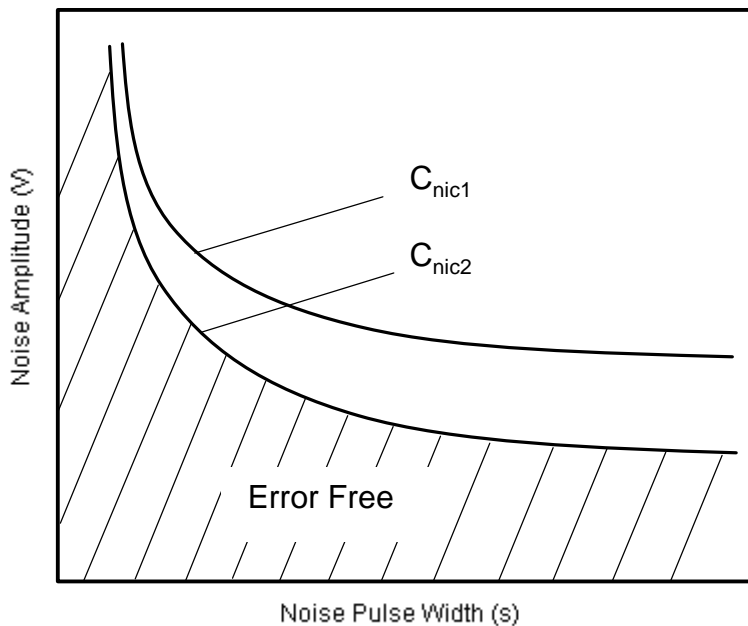
(a) Conventional domino

(b) Mirror technique

(c) NAND gate design



ANTE: A Noise-Tolerance Metric



Noise Immunity Curve

- Average Noise Threshold Energy

$$ANTE = E[V_{noise}^2 T_{noise}]$$

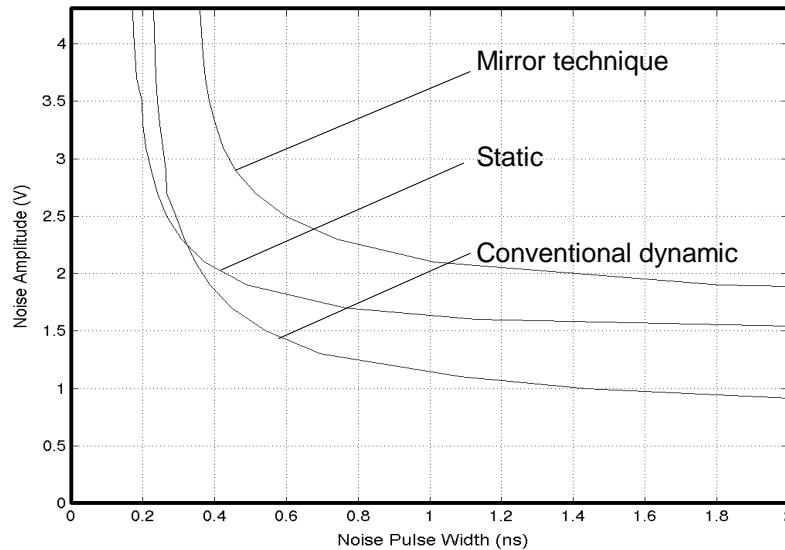
- Energy Normalized ANTE

$$NANTE = \frac{ANTE}{e}$$

e : Energy dissipated per cycle



Simulation Results: Full Adder



Design Specifications:

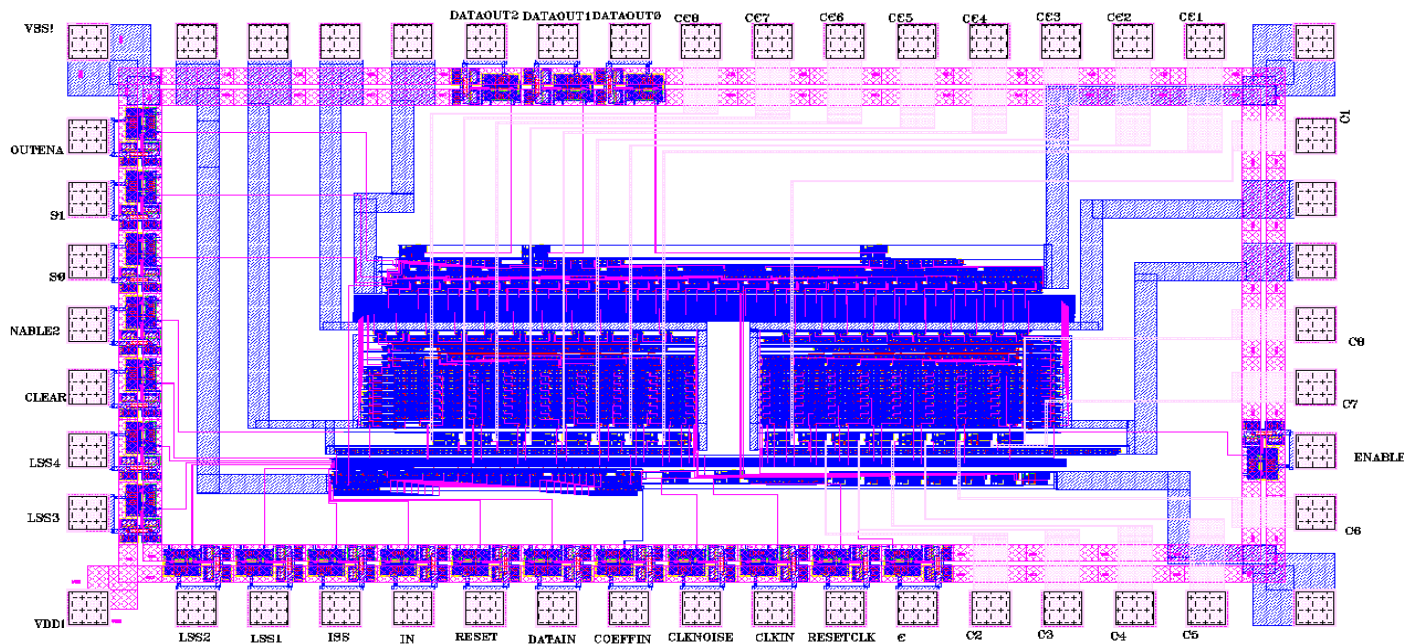
- (1) Power supply: 3.3V
- (2) Load capacitor: 20fF
- (3) Clock cycle: 1GHz

Technology: 0.35 micron CMOS

	Area (μm^2)	Energy (pJ)	ANIE (nJ)	Energy Normalized ANIE
Static	574.3	2.202	3.115	1414
Conventional dynamic	288.8	0.889	1.405	1580
Mirror tech.	487.2	1.693	5.203	3073



Noise-Tolerant ASIC



Technology: 0.35 μ m CMOS

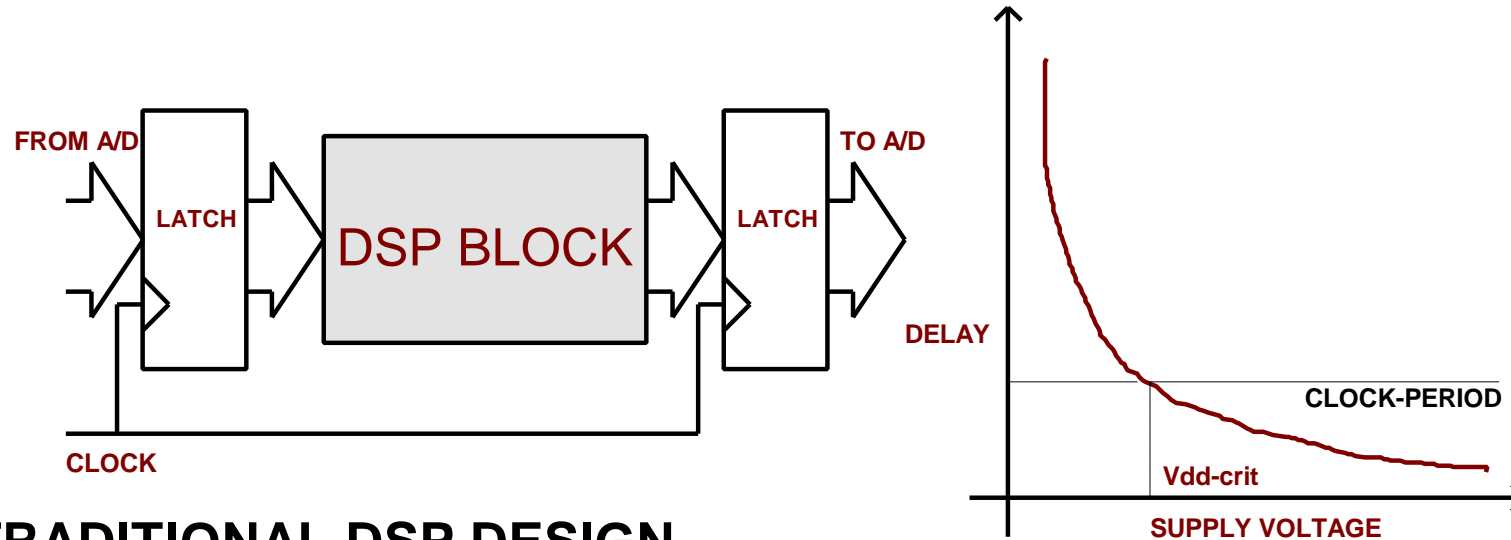
Pin #: 48

Transistor #: ~ 20K

Area: ~ 5mm²

Technique: dynamic, mirror noise-tolerant dynamic

Measured Noise immunity improvement: 34.1% ~ 69.5%, average: 55.2%



TRADITIONAL DSP DESIGN

- critical-path-delay of the DSP block < sample period.
- reduction in supply voltage to the DSP block is limited by $V_{dd-crit}$.

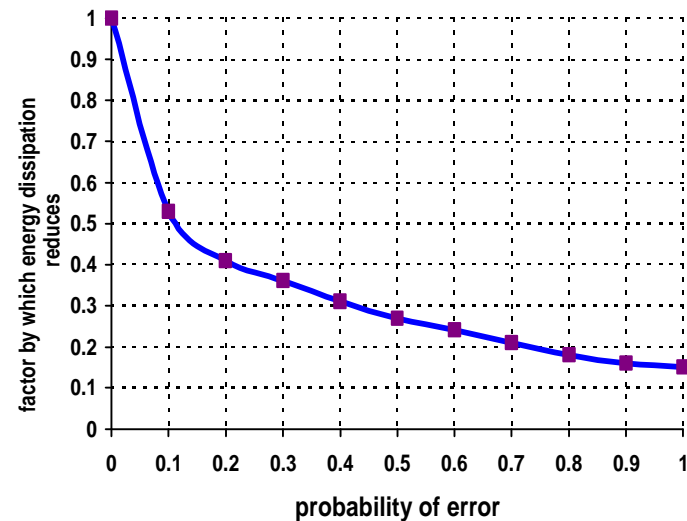
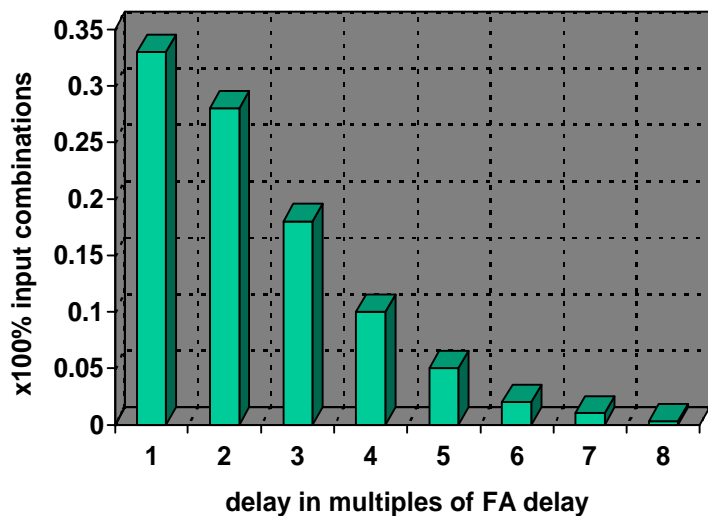
Soft DSP

- reduce V_{dd} beyond $V_{dd-crit}$.
- detect/correct errors in output via Algorithmic Noise-Tolerance.

MEET THE SNR/BER CRITERION AT REDUCED ENERGY DISSIPATION.

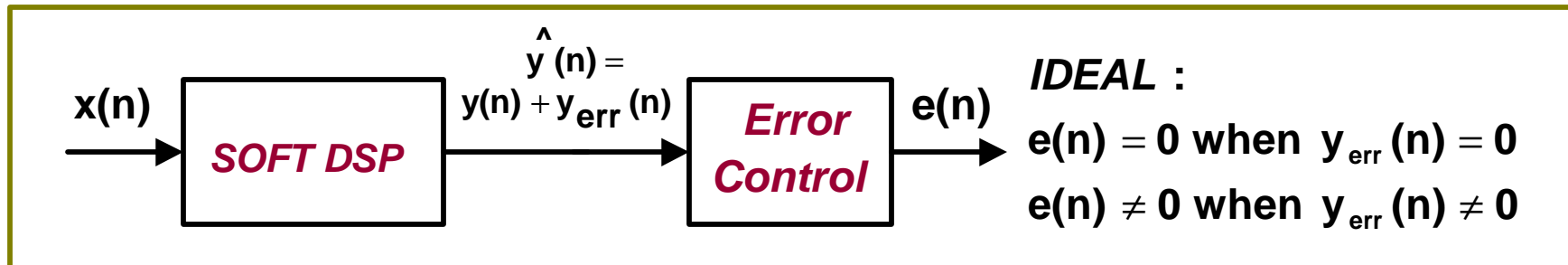
Error Probability in Arithmetic Units

PATH-DELAY DISTRIBUTION OF 8-BIT RIPPLE CARRY ADDER



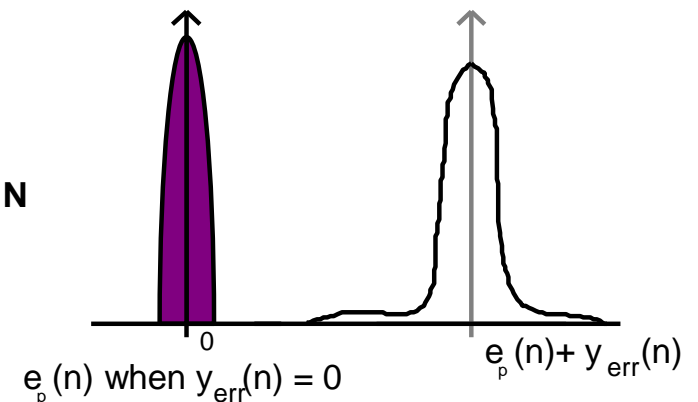
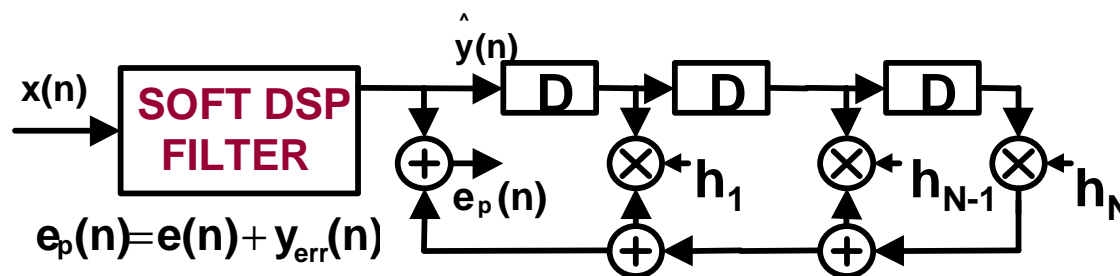
- 48% reduction in energy dissipation possible with prob. of err. = 0.1
- distribution with long tail leads to smaller error penalty
- errors at the AU level lead to SNR/BER degradation
- **Algorithmic Noise-Tolerance** to enhance performance

Algorithmic Noise-Tolerance (ANT)



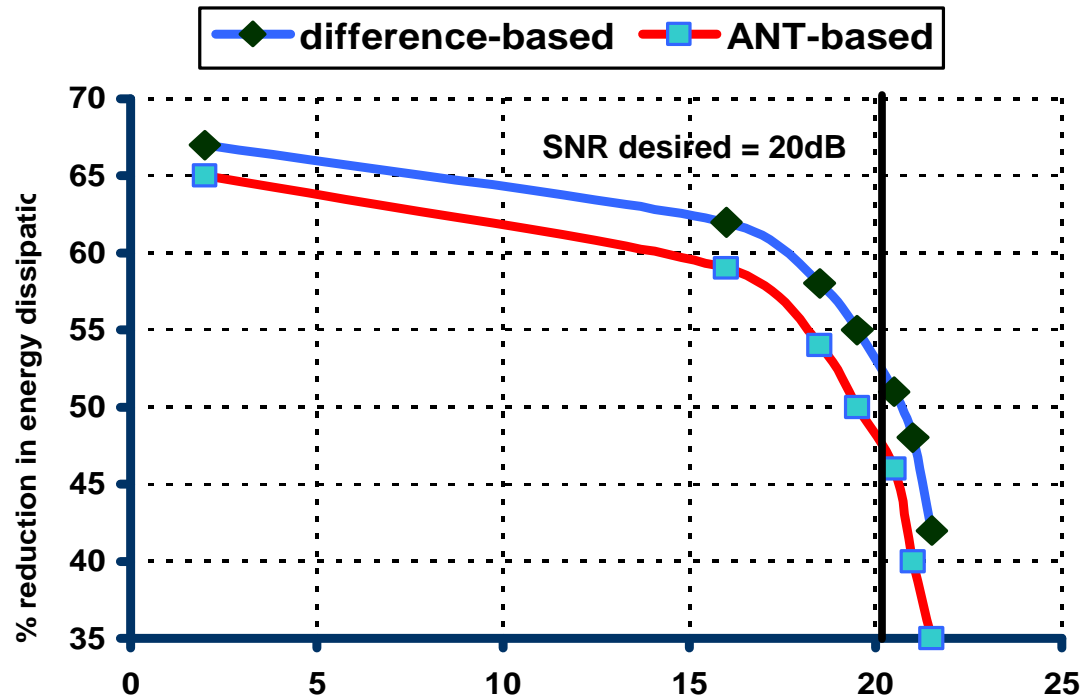
ANT via LINEAR PREDICTION:

- exploit the correlation in filter output to perform error-control
- optimum predictor for error detection - minimize MSE $e(n)$





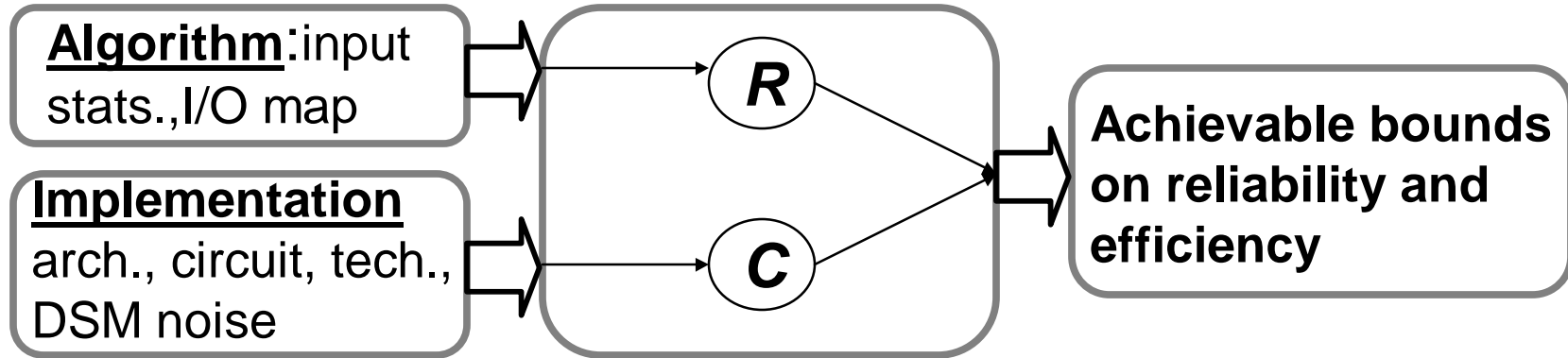
Frequency Selective Filtering via Soft DSP



- difference-based scheme : SNR at the filter output
 - 52% power savings with 1dB SNR loss (**effective for high correlation**).
- prediction-based scheme:
 - 44% power savings with 0.7dB SNR loss (overhead: 2-tap predictor)
 - **effective for low correlation** (higher BW).



Information-Theoretic VLSI Framework



- Information Transfer Rate: R (bits/sec)
- Information Transfer Capacity: C (bits/sec)
- For **reliability** : $C > R$; For **energy-efficiency**: $C @ R$

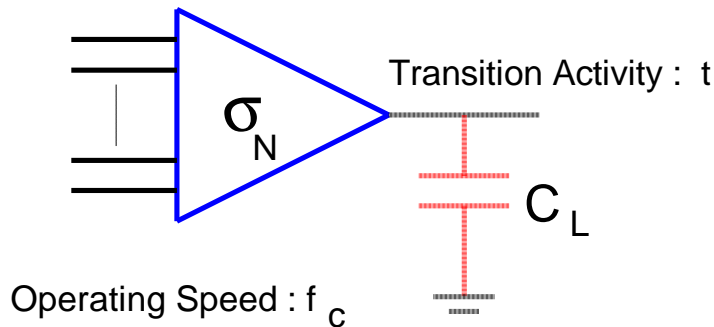
Soft DSP

- Projects:
 - Lower-bounds on energy-efficiency of noisy digital circuits (Hegde)
 - Lower-bounds on signal transition activity and coding schemes (Ramprasad, Prof. Hajj)
 - Bounds on: throughput and energy-efficiency; adaptive systems (Goel)
 - Design techniques for ultra efficient VLSI



Lower Bound on Energy Dissipation

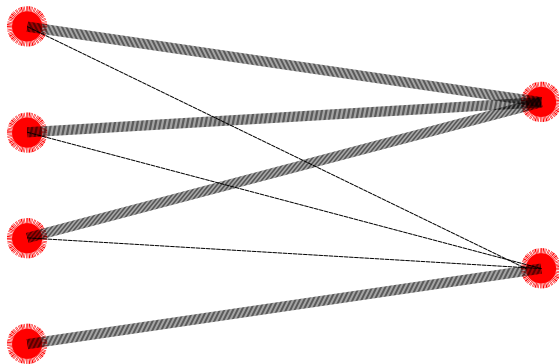
Information Transfer Rate : R



- Minimize:
 $E_b = (P_{dyn} + P_{stat})/R$ bits/sec

subject to:

$$C \geq R$$



----- e $1 - e$

$$e = Q(V_{dd}/2s)$$

- operating point:

$$f_c = k_m V_{dd} / C_L$$

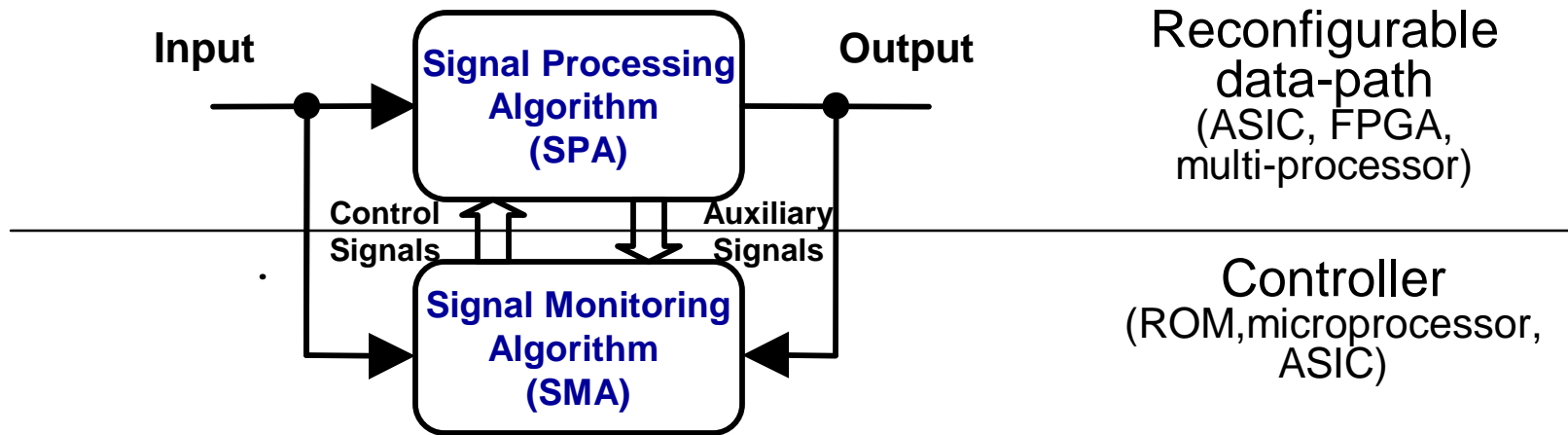


Dynamic Power

Energy dissipation at minimum supply voltage is **greater** than minimum achievable energy dissipation



Reconfigurable DSP

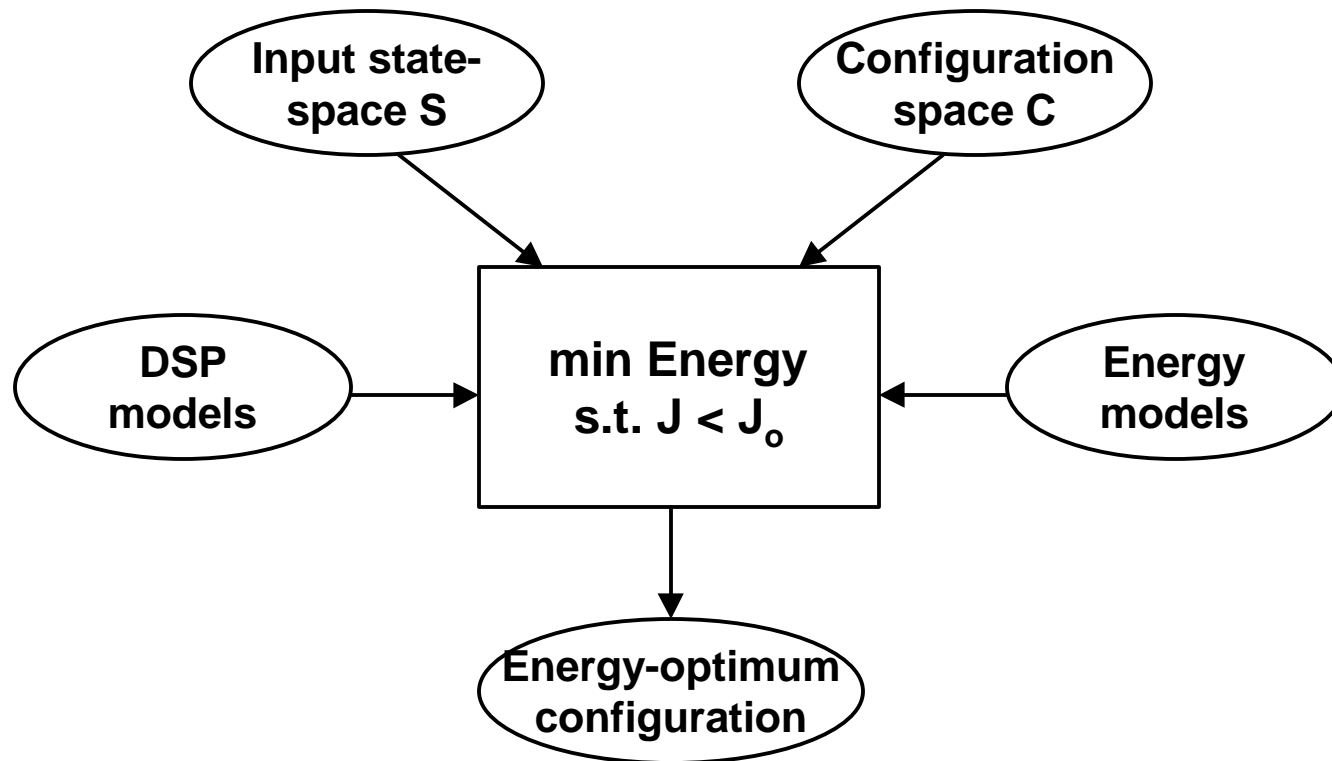


- Dynamic Algorithm Transforms: **min Energy/Throughput subject to: DSP constraint**
- Projects:
 - Low-power adaptive filtering, VDSL equalizer ASIC (Goel, Tschanz)
 - Domain-specific reconfigurable DSP processors (Tschanz)
 - Reconfigurable DSP for video processing (Minocha)
 - FPGA board design (Park)
 - Video over wireless (Profs. Jones and Ramchandran)



Dynamic Algorithm Transforms (DAT)

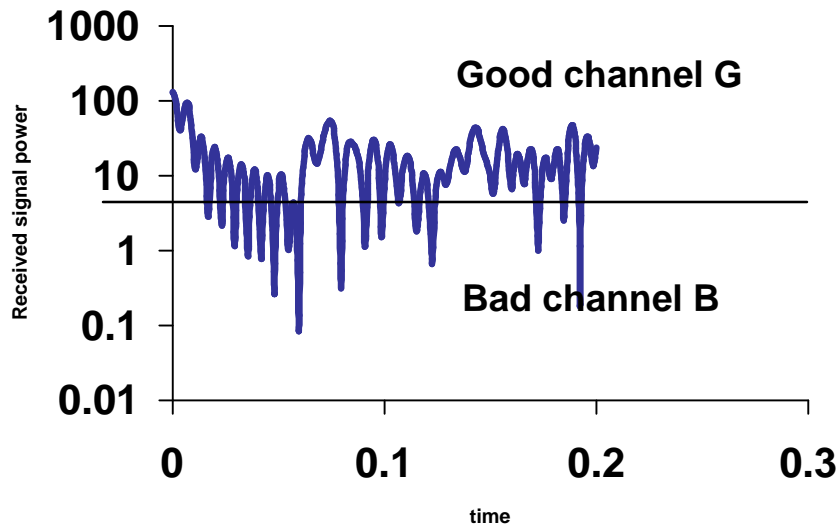
A framework for designing low-power
reconfigurable DSP systems



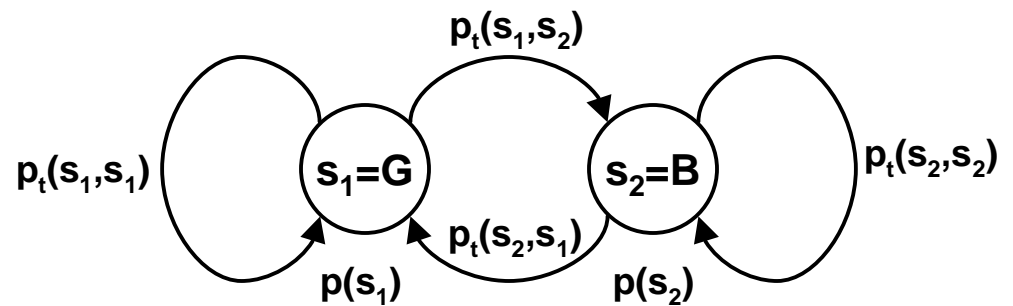


Input State-space S

- Set of all possible input states



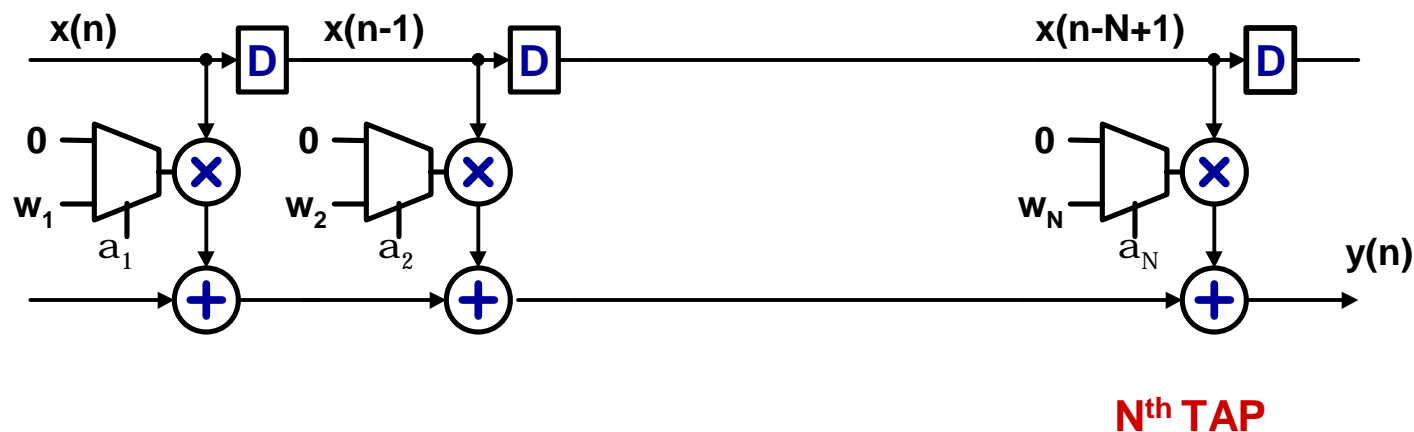
Signal power received at the mobile unit
 mobile speed = 60 miles/hr
 RF signal frequency = 2 GHz



- $s(n)$ = received signal power
- Two-state model
- State s_1 : Good channel
- State s_2 : Bad channel
- $p(s_i)$: steady-state probabilities
- $p_t(s_i, s_j)$: transition probabilities

Configuration-space C

- Set of all possible configuration vectors the reconfigurable datapath can support

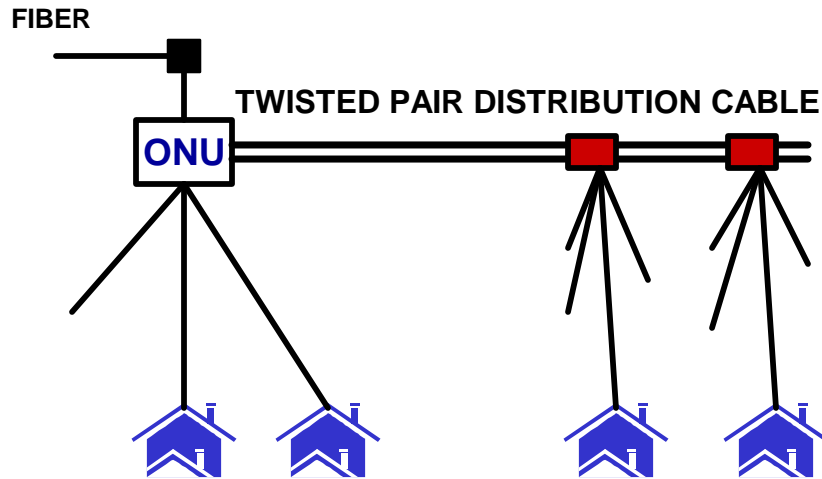


$c(n)=[\alpha_1, \alpha_2, \dots, \alpha_N]$: N-bit configuration vector

C: Set of all N-bit tuples (2^N vectors)



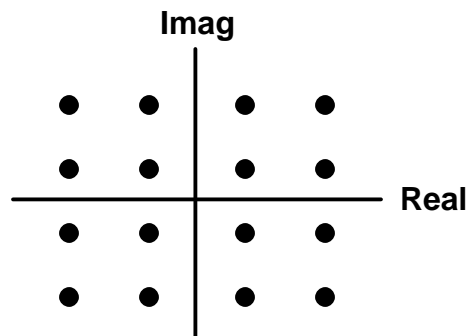
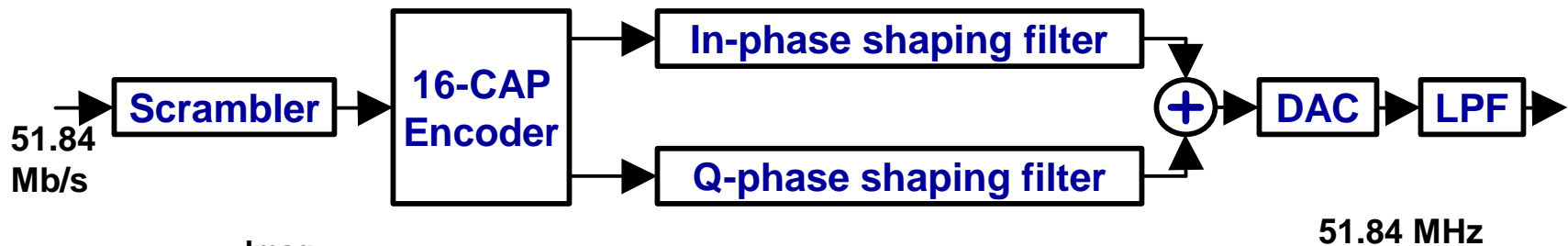
Very High-speed Digital Subscriber Loop



System	Data-rate	Distance
ADSL	1.544 Mb/s	18 kft
ADSL	8.448 Mb/s	9 kft
VDSL	12.96 Mb/s	4.5 kft
VDSL	51.84 Mb/s	1 kft

- Cable length
 - 100ft to 1kft (worst-case)
- Far-end crosstalk
 - 4-11 interferers
- Desired BER= 10^{-7}
 - SNR=21.5dB

51.84 Mb/s VDSL Transmitter



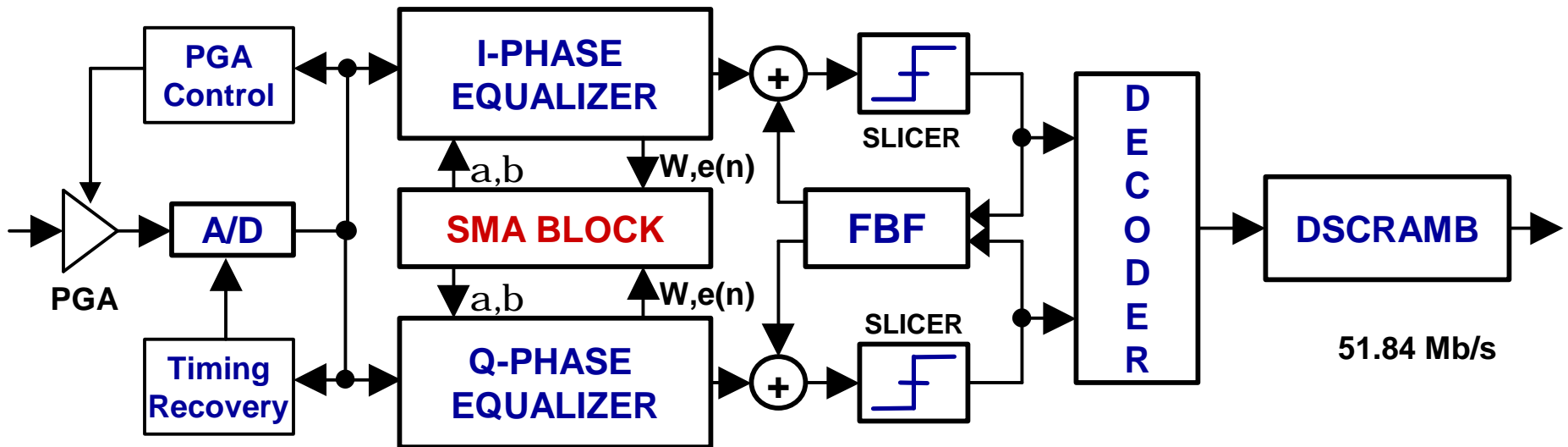
16-CAP signal constellation

- square-root raised cosine
- excess bandwidth=36%
- center frequency=12.96 MHz

Analog Front End

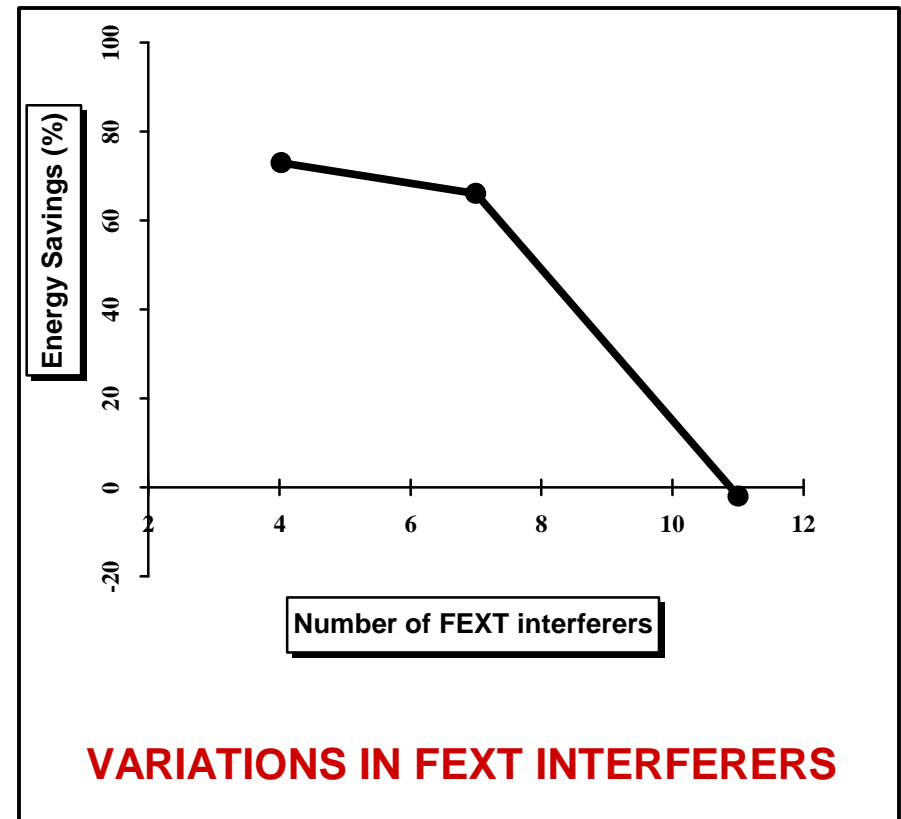
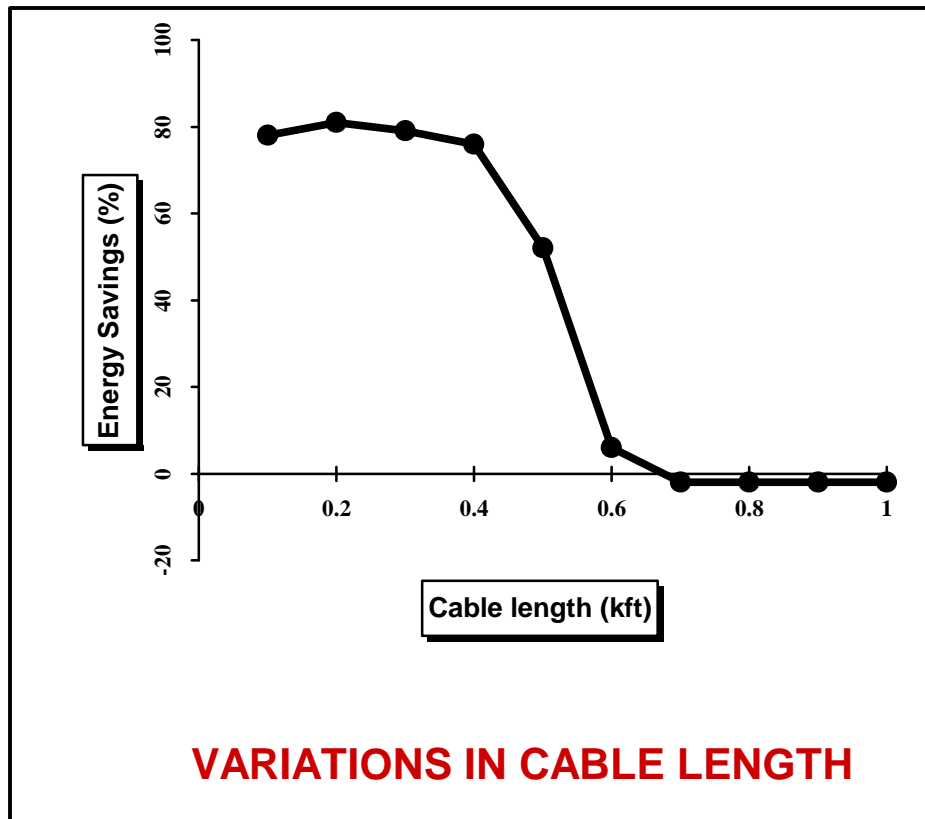


DAT-based 51.84 Mb/s VDSL Receiver



- I/Q-phase equalizers: 48 taps each
- FBF: 10 complex strength-reduced taps
- Powers of two LMS + Blind Equalization

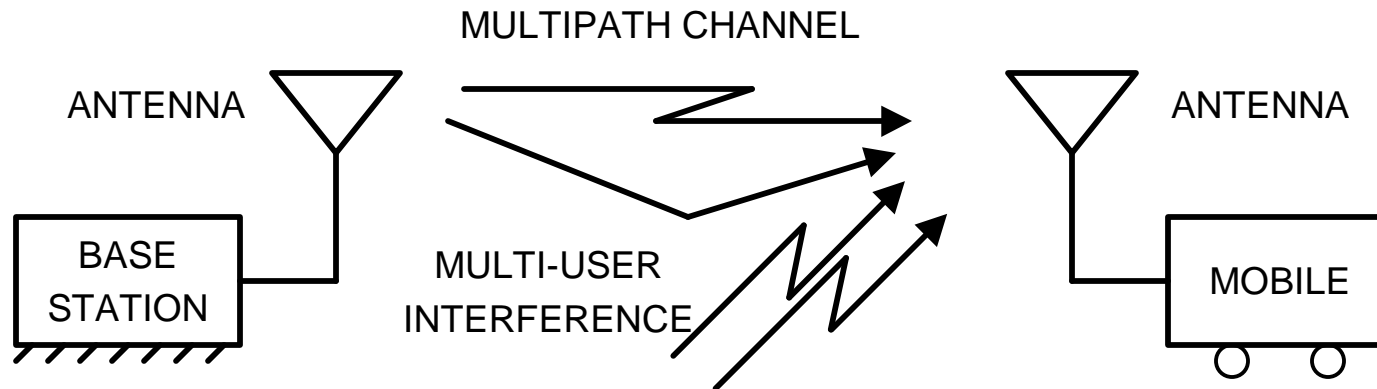
Energy Savings: 51.84 Mb/s VDSL



AVERAGE ENERGY SAVINGS=53%



Wireless Environment

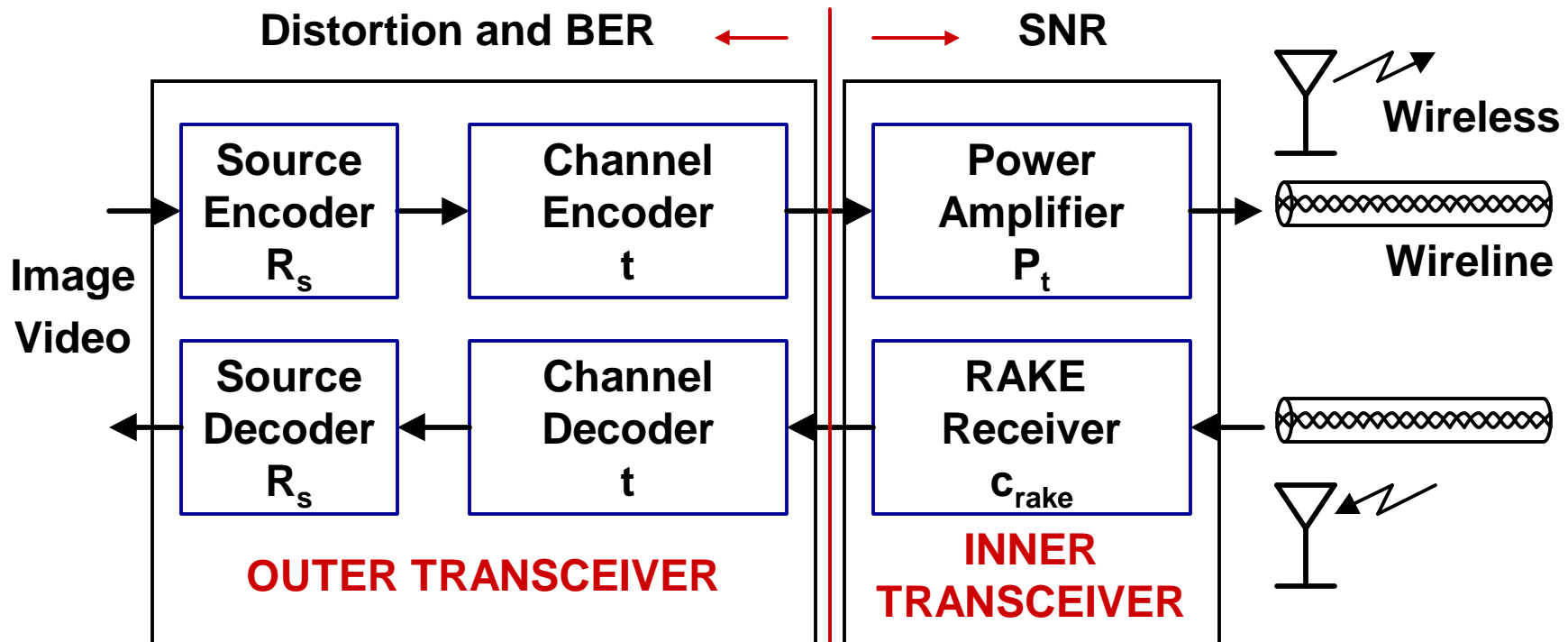


Flexibility Features of IMT-2000 systems

- Adaptability of system to time-varying propagation and traffic environments
- Adaptation to different spectrum allocations
- Ability to accommodate mixed-cell (pico, micro and macro) architecture
- Ability to handle different services: audio, video, speech, data, multimedia

Reconfigurable Wireless Communication System

- With Doug Jones and Kannan Ramchandran



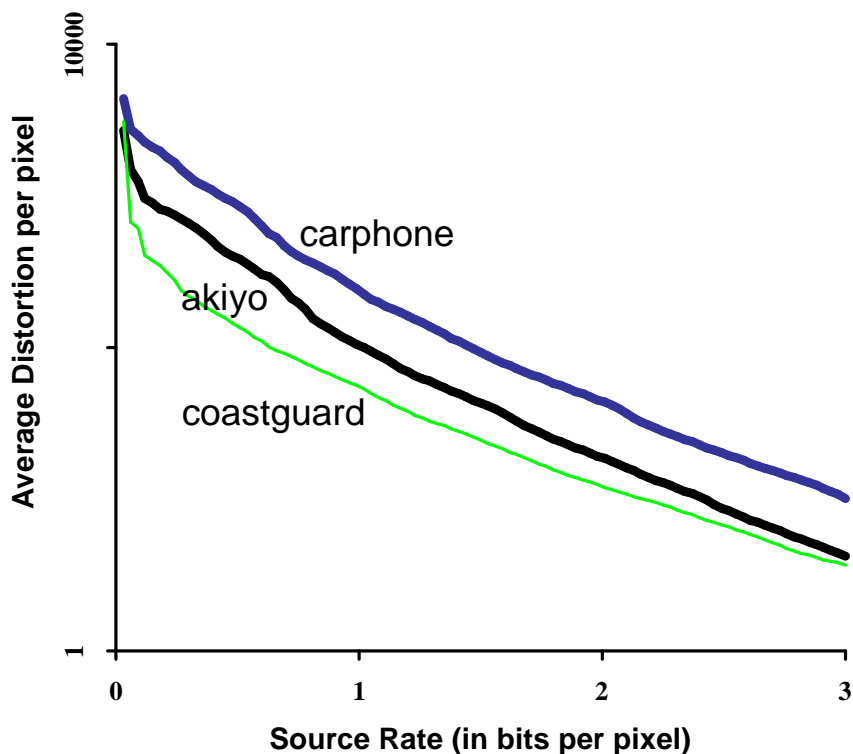
- Energy-optimum configuration via **Dynamic Algorithm Transforms** and **Joint Source-Channel Coding**

$$c_{\text{opt}}(s_i) = \arg \min \text{Energy}(c)$$

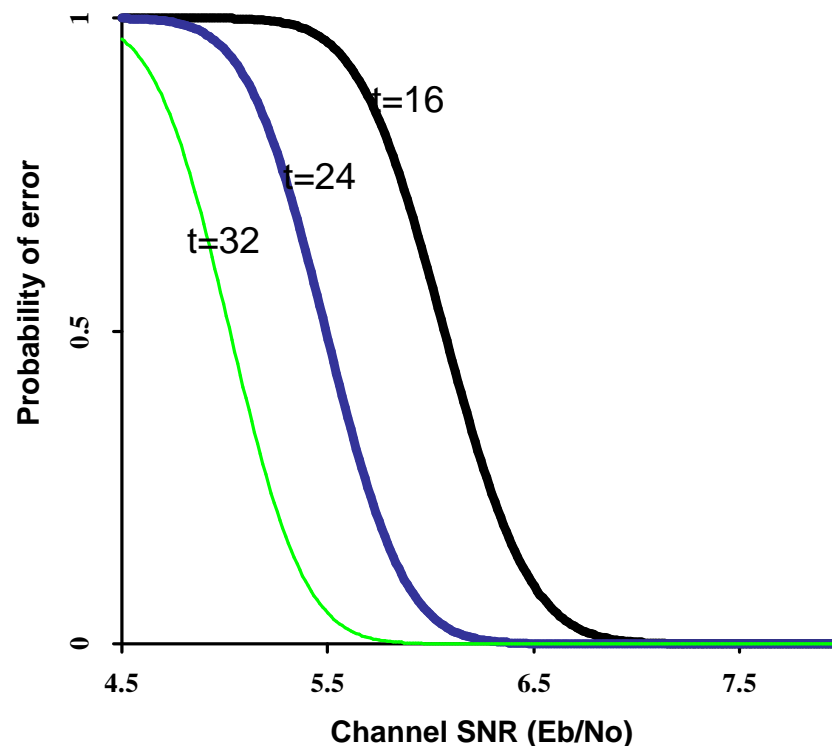
$$s.t. \begin{cases} D(c, s_i) < D_o \\ R_{\text{tot}}(c) < R_o \end{cases}$$



Source-Channel Variabilities

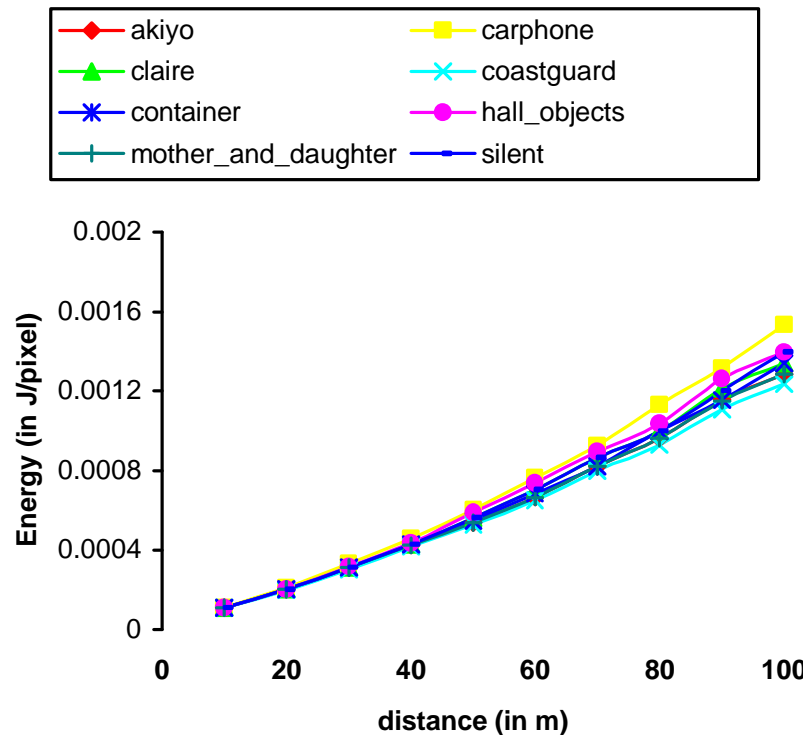


(Rate-Distortion Curves)
SOURCE VARIABILITIES

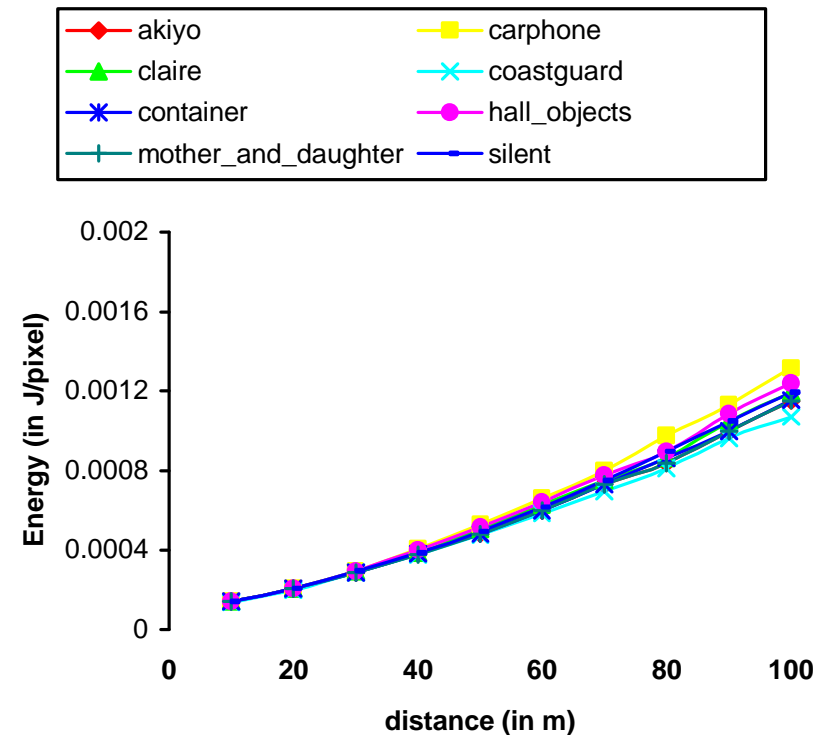


(BER Curves)
CHANNEL VARIABILITIES

Simulation Results: QCIF Images and IMT-2000 Test channels



Channel A (low delay spread)



Channel B (medium delay spread)

- Energy Savings: maximum 93% (average 59%)
- Fraction of Energy due to the digital blocks:
 - ranges from 40-10% (for distance: 10-100m)

Summary

- Evolving next generation (3G) wireless standards: **flexibility** and **energy-efficiency**.
- Evolving integrated circuit technology: **deep submicron noise**, **complex system-on-a-chip (SOC)**.
- **DSP via Soft Computations** (Soft DSP): energy-efficient, **noise-tolerant circuit design** and **algorithmic noise-tolerance**
- Dynamic low-power techniques are required
 - inter-application dynamism => domain-specific processors
 - intra-application dynamism => run-time reconfiguration
- **Dynamic algorithm transforms**: input space, configuration space, DSP models, energy models, joint-optimization of energy & performance