



3G Cellular Baseband Design

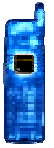
S. Sriram

(sriram@ti.com)

Wireless Communication Branch

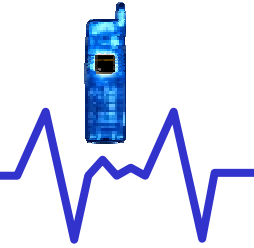
DSPS R&D Center, Dallas

Outline



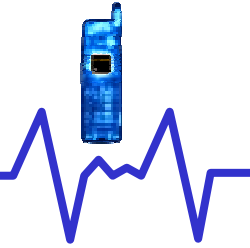
- Research activities in the Wireless Comm. Branch
- 3G Digital Baseband processing
- Coprocessor strategy
- HW/SW partitioning for handset and base station
- Useful low power techniques
- IC/MUD/Smart antenna extensions
- TI interaction with BWRC. Possible topics:
 - design/test/validation methodology and tools
 - reconfigurable architectures
 - ??? - discussion
- Summary

Wireless Comm Branch Research



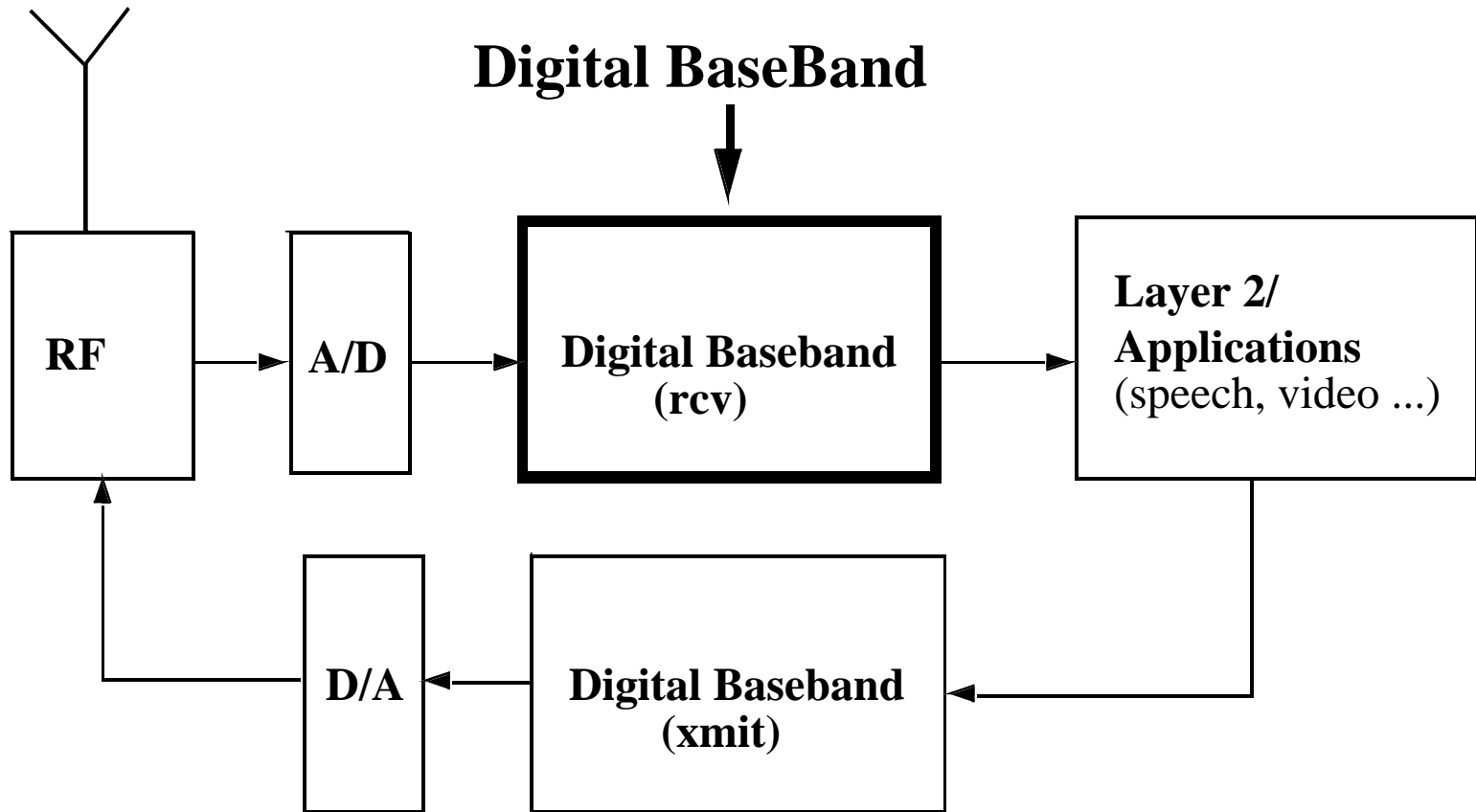
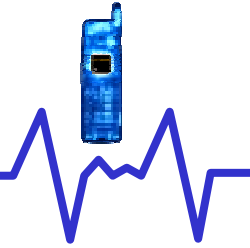
- Active in ARIB, ETSI and 3GPP for 2 years
 - Contributions to FDD mode
 - 3-stage acquisition using Cyclically Permutable codes, PSC & SSC definition
 - Power control bit positioning
 - Open loop transmit diversity, Closed loop transmit diversity
 - RACH preamble
 - Contributions to TDD mode
 - Acquisition using Cyclically Permutable codes
 - Open loop transmit diversity
 - Cell parameter cycling
- Bluetooth, High speed WPAN
 - Active in 802.15.3, Bluetooth 2
 - 40Mbps data rates

WCB Research (cont.)

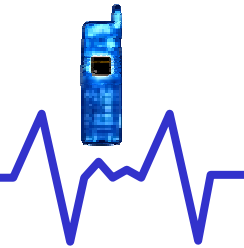


- **Coding**
 - Turbo Codes for 802.15.3
 - Proposed SCCC
 - Space-Time codes
 - Turbo trellis and LDPC for wireless applications.
 - Codes increasingly need to work with ARQ
- **VLSI Architectures for Wireless**
 - Correlator Coprocessor
 - Viterbi Coprocessor
 - Turbo Coprocessor
 - IC/MUD Coprocessor

Digital Base-Band Processing

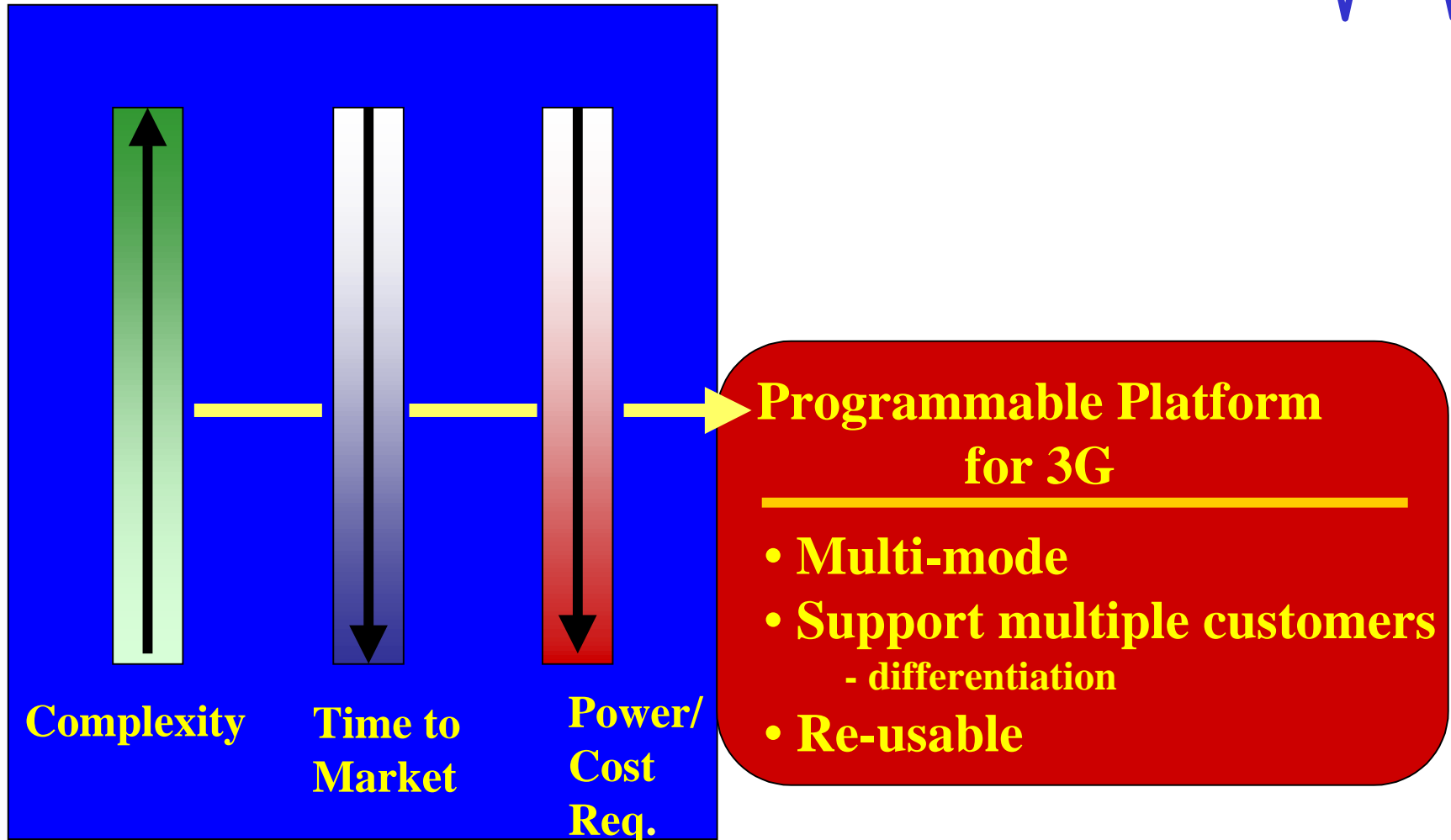
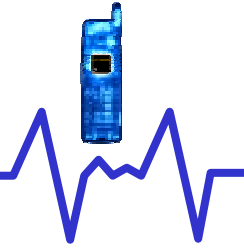


3G “Standards”

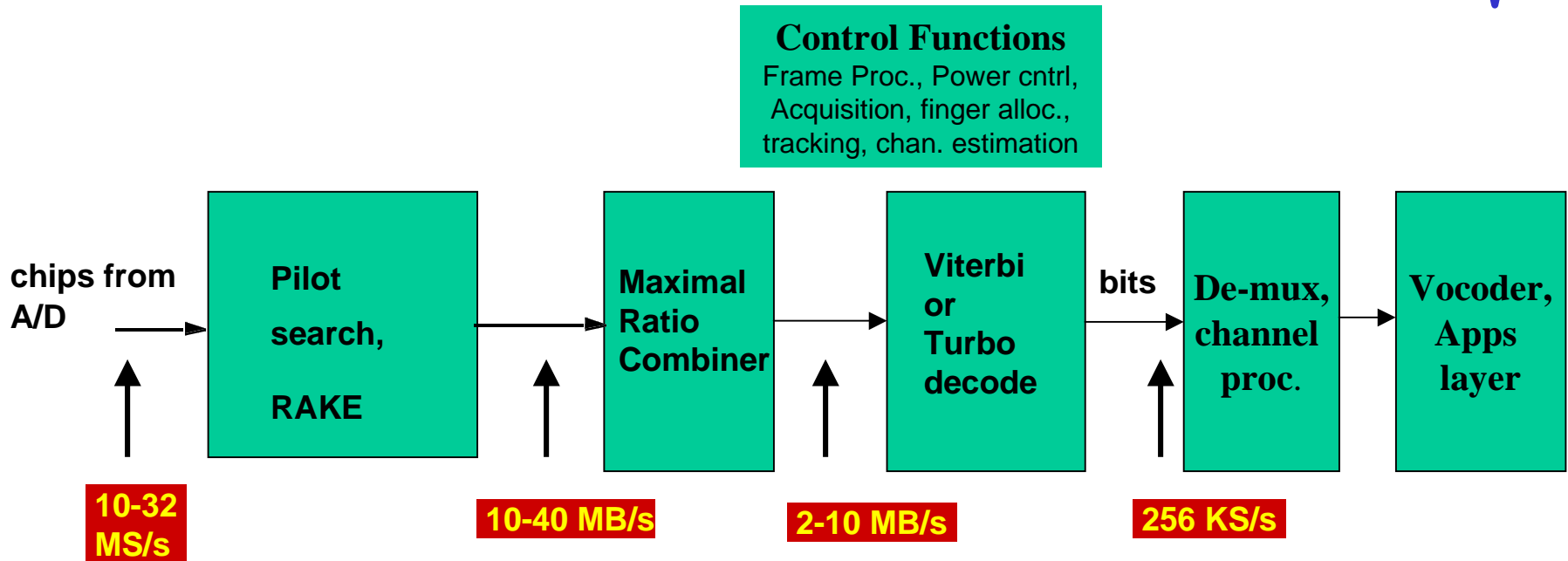
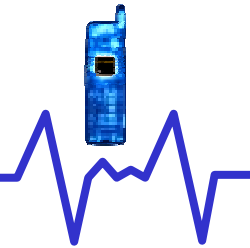


- IS-2000: IS-95 + Extensions
 - CDMA: 1.2288MHz chip rate (and multiples)
- Wideband CDMA (3GPP) technology
 - 3.84MHz chip rate
 - FDD/TDD mode
 - 8kbps - 2Mbps rates
- “2.5G” TDMA technologies: GPRS, EDGE
- Standards are more a toolset than a definition
 - CDMA, several GOPS processing / channel

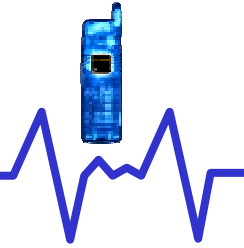
3G Design Challenges



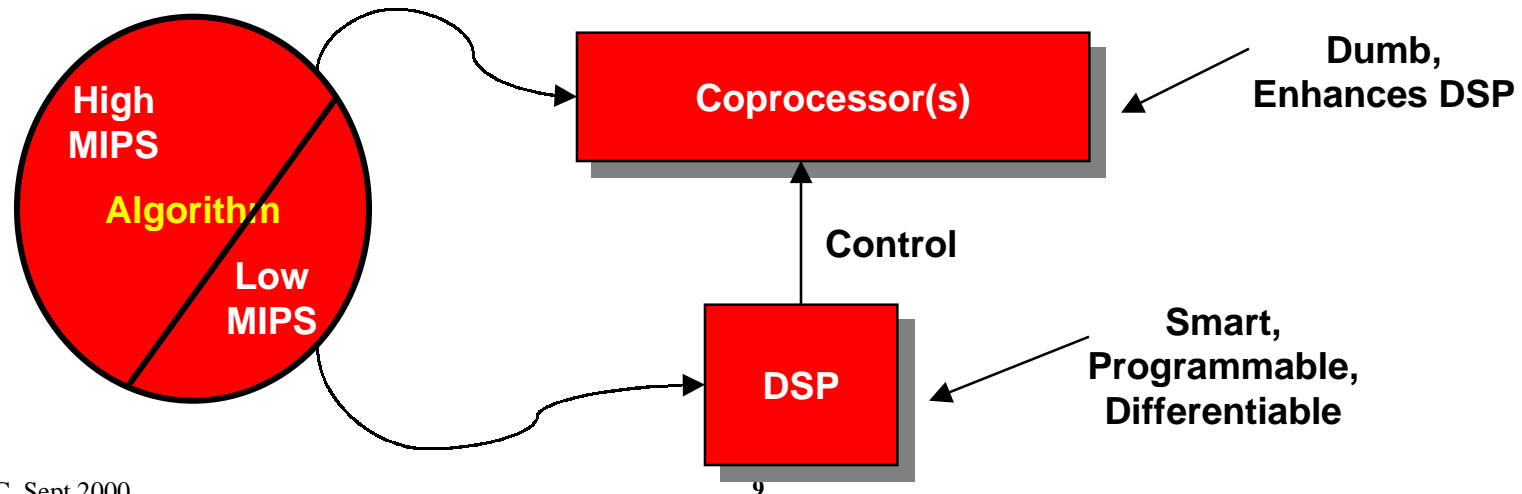
3G DBB Functionality



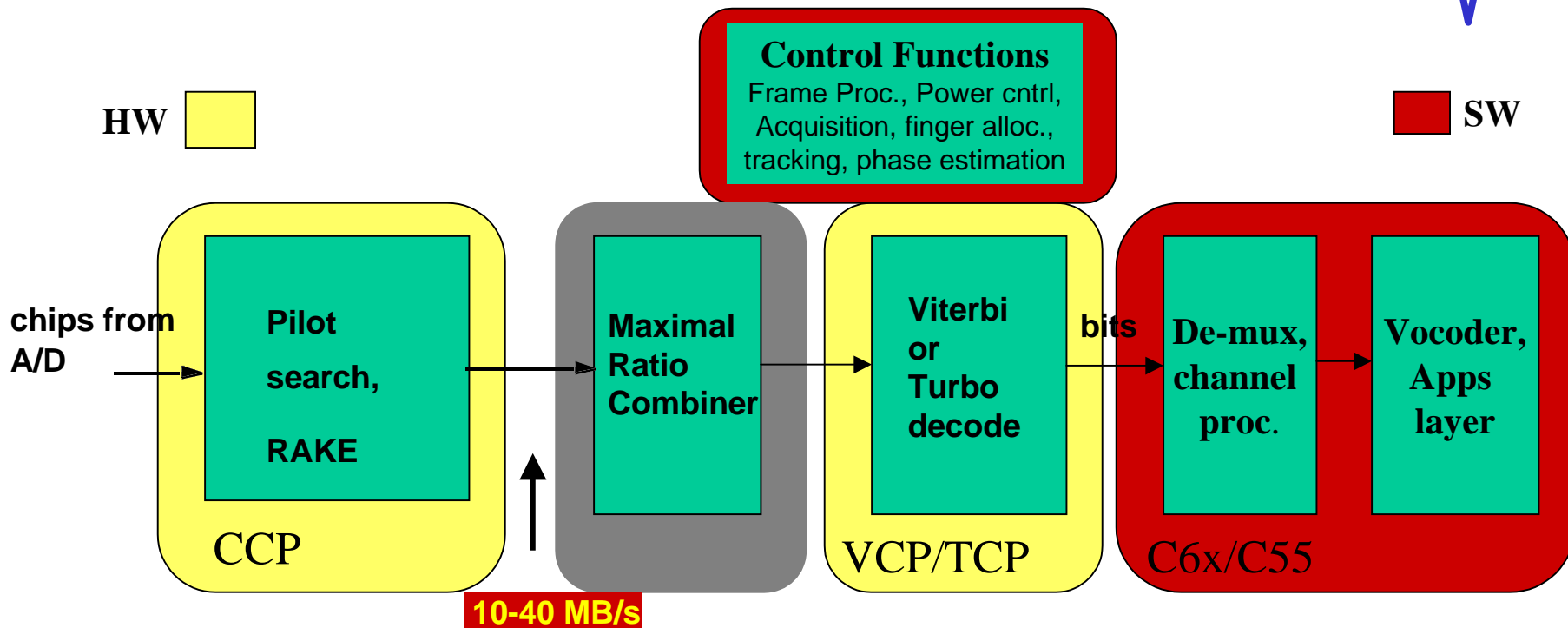
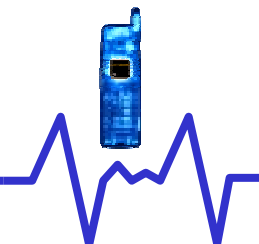
Coprocessor strategy



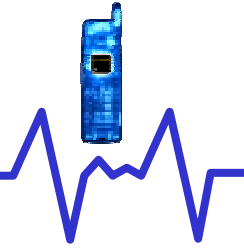
- HW assist for the high MIPS portions
- Use the DSP for low MIPS portions.
- DSP control of the “dumb” operations performed by the coprocessors
 - system is essentially fully programmable in the domain of interest.



HW/SW Partitioning

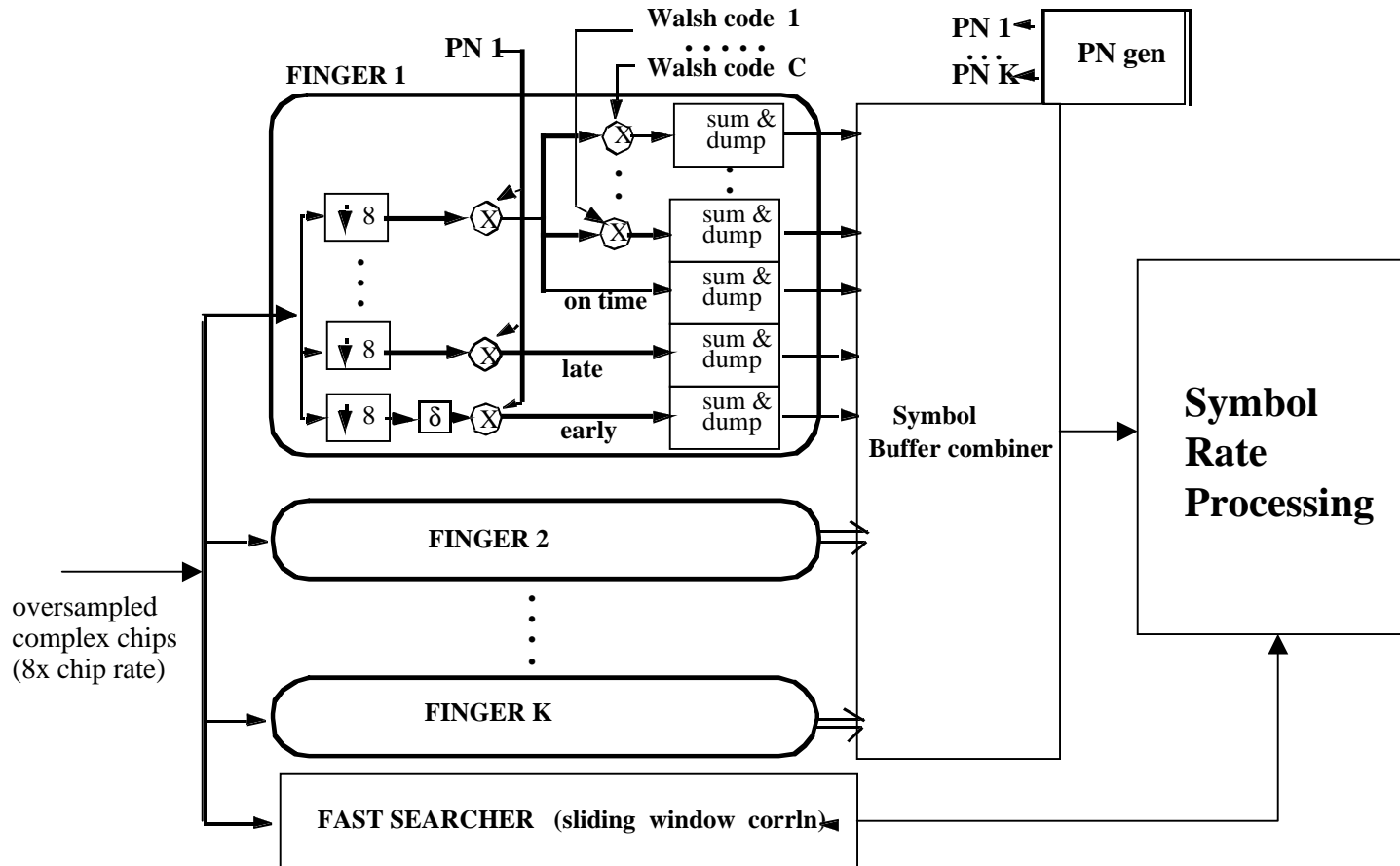
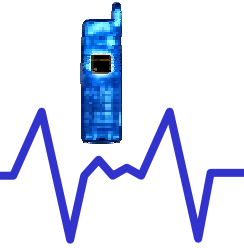


Loosely vs. Tightly Coupled CPs

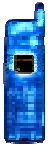


- Loosely Coupled CP
 - CP runs in parallel with DSP.
 - many cycles per instruction (subroutine call to hardware).
 - task based scheduling problem with interrupt or polling based synchronization.
 - Data passed is large blocks usually by DMA.
- Tightly Coupled CP
 - CP runs instead of DSP.
 - ISA enhancement.
 - no scheduling problem but no parallelism.
 - Data passed is a few words with access directly into CPU registers.

CDMA chip rate functions

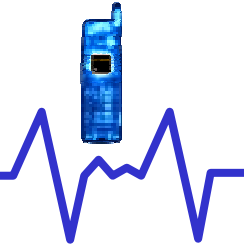


Correlator Coprocessor



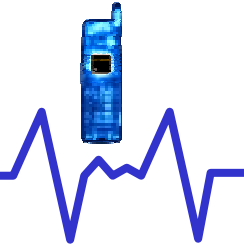
- **Applicable to cellular - mobiles & base stations, GPS**
- **Programmable to support various spreading factors & spreading schemes**
- **Multiple cellular standards**
- **Variable number of rake fingers, number of data channels/finger**
 - » **pool of correlation resources, may be flexibly allocated**
 - » **higher clock rate yields increased functionality**
- **Design tracks technology better: more like a CPU than ASIC**

Low Power Techniques



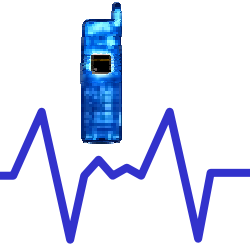
- Voltage scaling for throughput constrained systems
 - Architectural Parallelism
 - Avoid multiplexing of functional units/busses
 - maximally parallel design
 - Number systems
 - e.g. sign-magnitude
 - Bus encoding techniques
- Signal statistics not affected by muxing
 - CDMA input signal mostly noise
 - Registers can be consolidated into SRAM
 - Design flexibility
 - scalable
 - extensible
 - OK to sacrifice little power for more flexibility

Design methodology



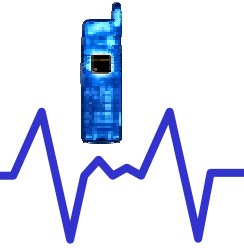
- Algorithm simulation: Matlab / SPW
- Gate count / Memory usage / Power estimation
 - Preliminary synthesis / Excel spreadsheet
- Performance simulation
 - Bus b/w, memory usage, dataflow between components
- Behavioral simulation of architecture (C)
- RTL simulation (VHDL)
- Post-synthesis / Gate level simulation
- Emulation using Quickturn/custom FPGA board

Tool features would like to see



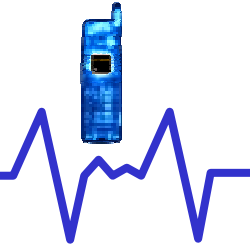
- Smart way of performing high level tradeoffs
 - Very useful: Excel with Gantt-chart type visualization
 - Is there a better approach??
- Hardware/Software co-design
 - Mostly obvious which part belongs in HW
 - In grey areas (e.g. MRC) the issues involved are
 - Interrupt rates and bandwidth to CPU
 - Memory requirements
 - Interface mechanisms and associated overhead

Tool requirements (cont.)



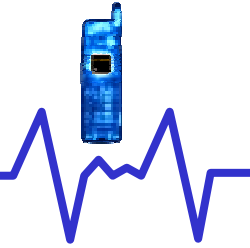
- RTL validation is still very time consuming
- Multichannel support
 - Given HW+SW solution for 1 channel, how to replicate for a 64 or 128 channel solution
 - multiprocessor issues
 - RTOS issues
 - Efficient multiplexing of functionality on HW; efficient scheduling of SW processes
 - Interrupt handling, deadline management

Advanced algorithms



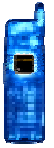
- Interference Cancellation
 - Multistage interference cancellation most promising
 - Extensions of Correlator Coprocessor to allow resreading and repeated desreading
- Multi-user Detection
 - MMSE based techniques
 - matrix inverse and matrix-vector multiplication
 - may apply this to short code (256 chips) option in 3GPP

Antenna array processing



- Transmit techniques
 - Smart spreader for transmit diversity
- Receiver techniques
 - Receive diversity
 - Space-Time rake combined with IC
 - handled by CCP/ICCP/C6x combination
 - DSP handles algorithmic variations
 - mechanisms for decision generation, channel estimation etc.

Summary



- 3G Cellular: multi-mode, complex
- Coprocessor based design
 - for handling multi-standard applications
- Identification and design of CPs a manual process
 - need to evaluate new system level design tools for assisting in SoC design
- Validation/testing is difficult, time consuming, ad hoc